HIGH PERFORMANCE CONTINUOUS-TIME FILTERS FOR INFORMATION TRANSFER SYSTEMS

A Dissertation

by

AHMED NADER MOHIELDIN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2003

Major Subject: Electrical Engineering

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Approved as to style and content by:

Edgar Sánchez-Sinencio (Chair of Committee)	José Silva-Martinez (Member)
Aydin Karsilayan (Member)	Kai Chang (Member)
Alexander Parlos (Member)	Chanan Singh (Head of Department)

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ABSTRACT

High Performance Continuous-time Filters for Information

Transfer Systems. (August 2003)

Ahmed Nader Mohieldin, B.Sc., Cairo University, Egypt;

M.Sc., Cairo University, Egypt;

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Vast attention has been paid to active continuous-time filters over the years. Thus as the cheap, readily available integrated circuit OpAmps replaced their discrete circuit versions, it became feasible to consider active-RC filter circuits using large numbers of OpAmps. Similarly the development of integrated operational transconductance amplifier (OTA) led to new filter configurations. This gave rise to OTA-C filters, using only active devices and capacitors, making it more suitable for integration. The demands on filter circuits have become ever more stringent as the world of electronics and communications has advanced. In addition, the continuing increase in the operating frequencies of modern circuits and systems increases the need for active filters that can perform at these higher frequencies; an area where the LC active filter emerges. What mainly limits the performance of an analog circuit are the non-idealities of the used building blocks and the circuit architecture. This research concentrates on the design issues of high frequency continuous-time integrated filters.

Several novel circuit building blocks are introduced. A novel pseudo-differential fully balanced fully symmetric CMOS OTA architecture with inherent common-mode

detection is proposed. Through judicious arrangement, the common-mode feedback circuit can be economically implemented.

On the level of system architectures, a novel filter low-voltage 4^{th} order RF bandpass filter structure based on emulation of two magnetically coupled resonators is presented. A unique feature of the proposed architecture is using electric coupling to emulate the effect of the coupled-inductors, thus providing bandwidth tuning with small passband ripple.

As part of a direct conversion dual-mode 802.11b/Bluetooth receiver, a BiCMOS 5^{th} order low-pass channel selection filter is designed. The filter operated from a single 2.5V supply and achieves a 76dB of out-of-band SFDR. A digital automatic tuning system is also implemented to account for process and temperature variations.

As part of a Bluetooth transmitter, a low-power quadrature direct digital frequency synthesizer (DDFS) is presented. Piecewise linear approximation is used to avoid using a ROM look-up table to store the sine values in a conventional DDFS. Significant saving in power consumption, due to the elimination of the ROM, renders the design more suitable for portable wireless communication applications.

DEDICATION

To my Parents,

To my Brother,

And to my fiancée Marwa

For their love and support

ACKNOWLEDGMENTS

First, I would like to express my sincere appreciation to my advisor, Professor Edgar Sánchez-Sinencio, for his guidance and support during my studies at Texas A&M University. His creativity, insight into circuit design, and keeping me to focus on the whole picture helped me a lot in my research. His energy and love of what he is doing inspires me a lot. I feel very grateful for his supervision both on the technical and the personal levels during my stay at College Station.

I would like to thank and acknowledge Dr. José Silva-Martínez. I enjoyed and learned much from the too many interesting technical discussions that I had with him. After any discussion, which normally take more than one hour, I thank him feeling embarrassed that I took a lot of his time but he always reply with his famous encouraging statement “you are always welcome”.

I am also indebted to Dr. Sherif Embabi, who provided a lot of precious advice during my internship at the wireless RF group of Texas Instruments.

I want also to thank my colleagues in the Analog & Mixed Signal Center for their friendship and all of their help over years. Mohamed Ibrahim and Mostafa Elmala make my moving to College Station more smoother than I predicted. They helped me a lot when I first arrived to start my studies at Texas A&M. Ahmed Emira, known as Ahmed^2, is more than a friend. On the technical level, we have worked closely together on more than two projects and the results were very fruitful. On the personal level, he is

like a brother for me. Ari Yakov Valero-Lopez and his wife Marcia Mendez-Rivera are great friends. My lab mate Sung Tae Moon is very helpful and helped making the lab a good place to work. Fikret Dulger helped me to speed up the start of my RF filter project and was very helpful in answering a lot of my technical questions. I had also the opportunity to work closely in the past year with the Chameleon team which includes Ahmed Emira, Ari Yakov Valero-Lopez, Sung Tae Moon, Alberto Valdes-Garcia, Bo Xia, and Chunyu Xin. I want to thank all of them. It is a great experience for me to work in a team, which I believe, will be very beneficial for me in the future. I want to wish best of luck to all of the newer students in the group.

Thanks also go to my committee members: Dr. Aydin Karsilayan, Dr. Kai Chang, and Dr. Alexander Parlos for their time and valuable comments on my research.

I want also to say, “thank you” to the secretary of our group: Ella Gallagher. Her incredible sense of humor improves a lot the working environment.

Special thanks to my parents Nader Mohieldin, Inas Abuzaid, my brother Ashraf, and my fiancée Marwa for their love and encouragement. I could not have completed this dissertation without it.

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CHAPTER I

INTRODUCTION

1.1. Motivation and Background

In any system that interfaces with the real world, the quantity to be measured and later processed is always contaminated with noise and interferes. A filter is usually used in order to get rid of the unwanted noise and reject the surrounding interferes. Although we are living in a digital age, any system that interfaces with the real world, i.e., the analog world, will find use for continuous-time filters. A typical digital processing system is shown in Fig.1.1. The physical quantity to be processed is converted to an electrical signal via a transducer. This signal is then converted to a digital signal via an analog to digital converter (ADC) for further processing by the digital signal processor (DSP).

According to Nyquist theory and to avoid aliasing, the input signal must be band-limited before the A/D conversion. This is achieved by a low-pass filter (anti-aliasing filter) that limits the bandwidth of the signal to half the sampling rate of the ADC. The processed digital signal coming out of the DSP is converted back to an analog signal via a low-pass reconstruction filter. Both the anti-aliasing filter and the reconstruction filter are analog filters operating in continuous-time.

This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

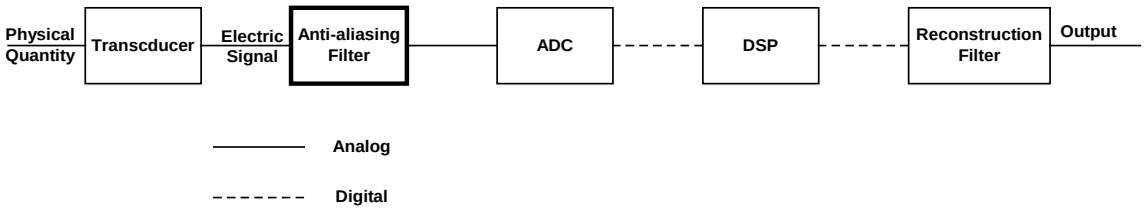

Fig. 1.1 A typical digital processing system

The term continuous-time is used in contrast to the term sampled-data. Sampled-data filters do not work with the digital representation of the signal samples, as digital filters do, they rather operate on samples of the signal itself. Thus these filters are discontinuous in time but continuos in processed data values. The best-known example of such an approach is that of switched-capacitor filters. Due to the sampling operation involved, continuous-time anti-aliasing filter and reconstruction filter are still needed in those kinds of switched-capacitor systems. Table 1.1 summarizes the properties of the previously discussed filter categories.

Table 1.1 Comparison of three types of filter categories

	Digital	**Sampled-data**	**Continuous-time**
Time samples	Discrete	Discrete	Continuous
Data samples	Discrete	Continuous	Continuous
Need anti-aliasing and reconstruction	Yes	Yes	No
Mathematical Description	Z-transform	Z-transform	S-transform (laplace)

Filters can be also categorized according to the relative size of the elements used with respect to the wavelength of the signal into two categories: distributed and non-distributed filters. In a non-distributed (lumped) filter, the physical dimensions of the used elements (resistance, inductance, or capacitance) are negligible compared to the wavelength of the fields associated with the signal. Thus they are considered as simple elements concentrated within the boundaries of the corresponding physical element. This is in contrast to the distributed filter, in which the physical elements have dimensions comparable to the wavelength of the fields associated with the signal and hence it is represented by a combination of physical elements.

The main focus of this research is the design issues of high frequency continuous-time integrated filters. High frequency continuous-time filters have been widely used, in recent years for various applications, especially for medium dynamic range applications, in cases where high speed and/or low power dissipation are needed. Those applications, as shown in Fig. 1.2, include video signal processing [1], hard-disk drive read channels [2], loop filters for phase-locked loops [3], and radio frequency wireless communication systems [4].

Using digital filters is not feasible for high frequency applications because they are very power hungry at high frequencies, i.e., power=$f_{clock}V^2_{DD}/2$. Although switched capacitor filters can have good linearity and dynamic range properties, they are not suitable for those kinds of applications either. This is mainly due to their limited ability to process high frequency signals due to the sampling operation. The sampling frequency should be chosen larger than the filter bandwidth to avoid inaccurate filter frequency

response. That requires the use of operational amplifiers (Op-Amps) with very wide bandwidths, to provide proper settling, demanding large currents; it is required that the unity gain frequency of the used operational amplifier be at least five times larger than the clock frequency used.

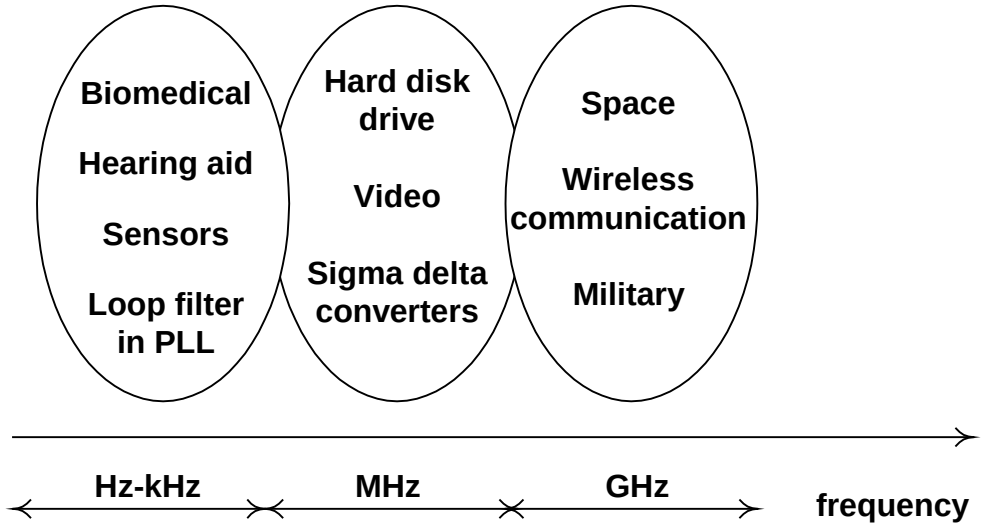

Fig. 1.2 A host of applications of filters

Thus continuous-time filters became the only option in these types of applications. Continuous-time filters include two main categories: passive filters and active filters. A passive filter has all of its elements passive. Therefore, a passive filter may include among its elements resistors, capacitors, inductors, transformers. If the elements of the filter include amplifiers or negative resistances, this is called active.

1.2. Passive Filters

The passive filters are those which do not employ transistors. Those include three main topologies: RLC filters, acoustic filters, and MEMS filters.

1.2.1 RLC Filters

Classic RLC filters built with resistors, inductors, and capacitors are still much in use in today's systems. They were first used to meet the needs of the early voice applications from the early 1920s. Although high performance on-chip resistors and capacitors can be fabricated in one or more forms in all IC processes, the performance of on-chip inductors is still unsatisfactory in silicon processes. This renders RLC filters unsuitable for implementation in an integrated form in silicon technologies.

In the microwave range (>1GHz), traditional passive microwave filter structures have been used. They use stubs as building elements [5], which require large area, and is not desirable in monolithic microwave integrated circuits (MMICs). Using couplers to realize filters allow for smaller area, where coplanar waveguides are widely used. There has been an increasing interest in realizing filters on MMICs. MMIC filters are typically used where they are required as part of another function which is implemented on MMIC. Inductors are designed routinely in a GaAs MMIC operating at several GHz.

1.2.2 Acoustic Filters

Surface acoustic wave (SAW) filters are applied extensively in today's communication equipment. These high performance components have reached a key

position in current communication technology assisting the efforts to increase the spectral efficiency of limited frequency bands for higher bit rates.

A SAW filter consists of a piezoelectric substrate with metallic structures, such as inter-digital transducers (IDTs), as shown in Fig. 1.3(a), and reflection or coupling gratings deposited on its plain-polished surface. It is based on propagating and/or standing micro-acoustic waves. Triggered by the piezoelectric effect, a microwave input signal at the transmitting IDT stimulates a micro-acoustic wave that propagates along the surface of the elastic solid [6]. The associated particle displacement of this SAW is bounded in the vicinity of the surface only. Vice versa, a SAW generates an electric charge distribution at the receiving IDT, causing a microwave electrical output signal to occur. The frequency response, shown in Fig. 1.3(b), of the SAW filter can be obtained form the Fourier transform of this charge distribution on its fingers.

During the last decade, driven by booming wireless technology business, great and important progress in SAW device performance was made, and a variety of innovative applications were developed. These developments are based on technological improvements. SAW technology has evolved to the GHz range in recent years and now routinely covers the frequency range up to 3GHz. This frequency band is used as carrier frequency for many new wireless communication and sensor applications.

SAW filters are not suitable for monolithic implementation and are usually implemented off-chip since silicon is not a piezoelectric material. Some attempts can be found in the literature [7] that implements an integrated SAW filter using a ZnO-SiO_2-Si layered structure. The aluminum inter-digital transducers are located at the ZnO-SiO_2

interface to obtain a high piezoelectric material combining the attractive SAW propagation with a relatively easy fabrication process. The reduced size and weight of the complete system will be an advantage in cordless telephone, car radio, and all kinds of portable consumer electronics product. Moreover, receiver architectures, such as in radio, television, and other telecommunication systems use higher IF frequencies to improve the interfering signal rejection.

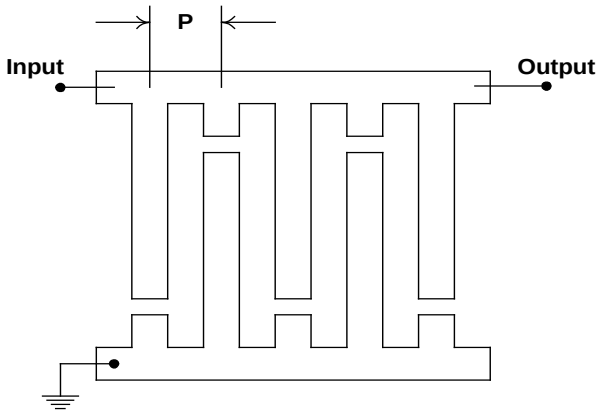

Fig. 1.3(a) Schematic of an integrated transducer with pitch p

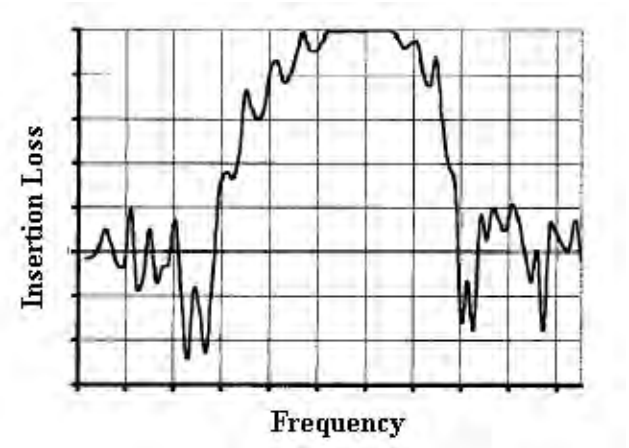

Fig. 1.3(b) Frequency response of a SAW filter

Traditional SAW filters satisfy the requirements of flat passband, sharp cutoff frequency response and high reliability. However one major problem with these devices is that they generally have high insertion loss. Several low loss filter techniques have been reported [8]. The relative bandwidths of most of these techniques are limited to below 5% with insertion loss of about 4dB and passband ripple of 1dB. However to serve the increasing number of users with a given communication system one will finally have to suppress more channels and therefore increase the bandwidths in both the transmitter and the receiver paths.

1.3. Active Filters

Significant attention has been paid to active continuous-time filters over the last three decades. Tens of thousands of journal articles and conference papers must have been published and presented over the years. The changes in technology have required new approaches. Thus as cheap, readily available integrated circuit operational amplifiers (OpAmps) replaced their discrete circuit (based on vacuum tubes), it became feasible to consider active-RC filter circuits using large numbers of OpAmps, and new improved architectures emerged.

Similarly the development of integrated operational transconductance amplifiers (OTA) led to new filter configurations which reduced the number of resistive components, and allowed transconductance-mode rather than voltage-mode. This gives rise to OTA-C filters, using only active devices and capacitors, making it more suitable for integration.

The demands on filter circuits have become ever more stringent as the world of electronics and communications has advanced. For example, greater demands on bandwidth utilization have required much higher performance in filters in terms of their attenuation characteristics, and particularly in the transition region between passband and stopband. This in turn has required filters capable of exhibiting high quality factor but having low sensitivity to component changes, and offering dynamically stable performance. In addition, the continuing increase in the operating frequencies of modern circuits and systems, increases the need for active filters that can perform at these higher frequencies; an area where the Q-enhanced LC active filter emerges.

1.3.1 Active-RC Filters

Active-RC filters have been around for some time as a means of overcoming the disadvantages associated with low-frequency passive RLC filters (of which the use of inductors is one). They offer the opportunity to integrate complex filters on-chip, and do not have the problems that the relatively bulky, lossy, and expensive inductors bring in particular their stray magnetic fields that can provide unwanted coupling in a circuit or system [9].

The Sallen and Key [10] circuit (which uses a voltage amplifier, resistors, and capacitors) is one of the most popular and enduring active-RC filter architectures. It has been around for about 48 years, yet research into active-RC filters still proceeds after all that time.

Active-RC filters have been widely used in various low frequency applications in telecommunication networks, signal processing circuits, communication systems,

control, and instrumentation systems. However, they cannot work at higher frequencies due to OpAmp frequency limitations and are not suitable for full integration if large resistors are required. They are also not electronically tunable and usually have complex structures. The most successful approach to overcome these drawbacks is to replace the conventional OpAmp in active-RC filters by an OTA giving rise to OTA-C filters. Programmable high-frequency active filters can therefore be achieved by incorporating the OTA. OTA-C filters also have simple structures, and can operate up to several hundreds of MHz.

1.3.2 OTA-C Filters

In recent years OTA-based high frequency integrated circuits, filters and systems have been widely investigated. This is due to their simplicity, electronic tunability, and suitability for high frequency operation due to open loop configuration.

The OTA has been implemented widely in CMOS and bipolar and also in BiCMOS and GaAs technologies. The typical values of transconductances are in the range of tens to hundreds of μS in CMOS and up to mS in bipolar technology. The CMOS OTA, for example, can work typically in the frequency range of 50MHz to several 100MHz. Linearization techniques make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent.

Although OTA-C filters have the potential to operate at relatively high frequencies (MHz range), the linear signal range of the used transconductance limits the dynamic range. Also the OTA-C filters become very power hungry at GHz range. Furthermore,

the frequency dependence of transconductance, sensitivity to parasitics becomes very prominent giving rise to the need of Q-enhanced LC filters.

1.3.3 Q-enhanced LC Filters

The market for mobile communication systems is rapidly expanding. One of the major aims of modern cellular radio systems is to provide high quality radio performance with low-power, small-size, small weight mobile telephones. To avoid degradation of system performance, the RF filters must have both low insertion loss and high selectivity.

At those RF frequencies, using LC filters becomes necessary to meet the performance requirements. The area required by the inductor becomes reasonable. Besides, they offer better dynamic range and power consumption than their active counterparts especially for high Q applications, which is usually the case in bandpass filters used in wireless communications systems.

Due to the losses associated with integrated spiral inductors implemented in standard technologies, the achievable quality factor in the RF range is limited. Hence to implement on-chip narrow band LC filters and to provide acceptable image rejection, when the filtered signal is down converted to IF, Q-enhancement is applied to compensate for the LC tank losses.

1.4. The Approximation Problem

Solution of the approximation problem is a major step in the design procedure of a filter. It is through the solution of this problem that the filter designer determines the

filter function, the response that satisfies the specifications. In practice, the specifications of a low pass filter are often given in terms of the cutoff frequency the maximum allowable deviation (error) in the passband, the stopband edge frequency, and the minimum attenuation in the stopband. In general, from those specifications, one is able to draw a frequency response magnitude plot. This plot can be approximated by a function that is then implemented using a low pass filter.

The approximation problem has been solved mathematically in various ways. Some of the best known and most popular lows pass functions in the frequency domain for magnitude responses are: Butterworth, Chebyschev, Elliptic functions, and Bessel-Thomson function for phase response. With the aid of any of the computer programs that are available nowadays, such as Fiesta-II [11], one can obtain the appropriate approximating function for any particular specifications. Then, since these functions are low pass, a suitable frequency transformation is applied in order to obtain high pass, band pass, or band stop filters according to the requirement [9].

1.5. High Order Filters

In most cases, the selectivity that is provided by a second order filter is not sufficient. Higher order filters are needed in order to satisfy the tough selectivity requirements in telecommunication systems, and many other applications. There are two main approaches to realize a high order filter; (1) to cascade second order stages without feedback (Cascade) [12] or through the application of negative feedback [13] (multiple-loop feedback MLF), and (2) simulation of passive LC ladder filters [14].

1.5.1 Cascade

In this approach biquadratic second order sections are cascaded and the high order function is realized as the product of biquadratic factors. These sections are simply cascaded by connecting the output of each section to the input of the following one. This method has the advantage of simplicity in designing the filter, provided that the output of each section is very low impedance or the input of each section is very high impedance.

1.5.2 Multiple-loop Feedback

In this approach multiple feedback is applied in a cascade connection of biquadratic sections. This leads to a better sensitivity performance of the overall circuit compared to the corresponding circuit obtained using the Cascade approach [9]. This approach has two general topologies: the leapfrog topology, and the summed-feedback topology.

1.5.2.1 Leapfrog Topology

Fig. 1.4 shows the leapfrog topology, where $t_i(s)$, i=1:m, are the second order biquadratic sections and f are the gain factors. This topology is useful in the functional simulation of an LC ladder filter.

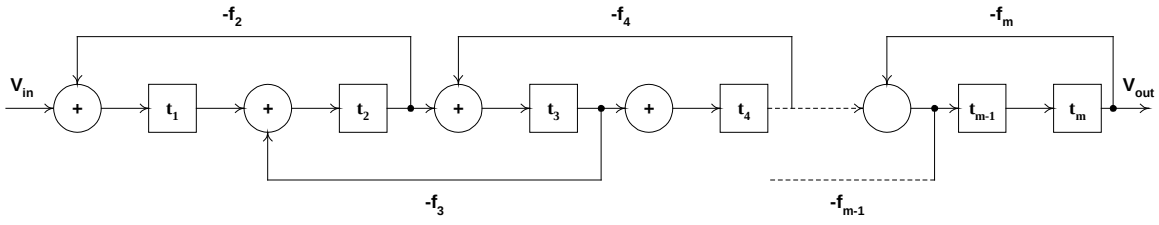

Fig. 1.4 Leapfrog topology

1.5.2.2 Summed-feedback Topology

The summed-feedback topology, as shown in Fig. 1.5, is not suitable for realizing any finite transmission zeros. To overcome this problem, one of two techniques can be used: (1) the multiple-or distributed-input technique, in which the input signal is also fed to the input of all cascading sections, or (2) the summation of the input signal and the output signals from all cascaded sections.

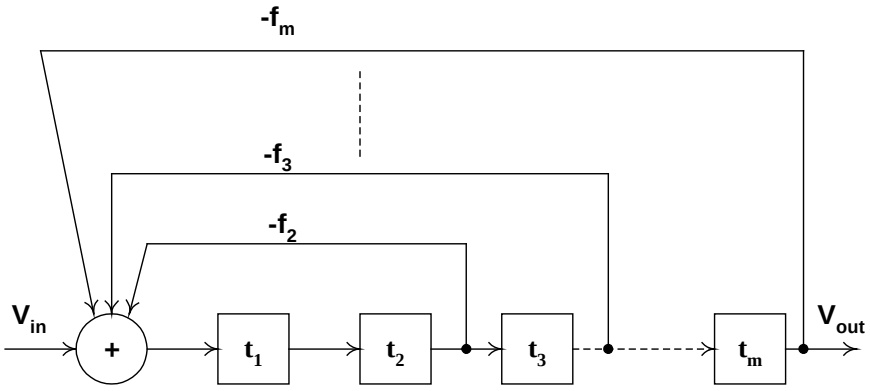

Fig. 1.5 Summed-feedback topology

There are three other design methods based on that topology: the primary-resonator block (PRB) [15] where all the used $t_i(s)$ stages are identical, the follow-the-leader feedback (FLF), and the shifted-companion form (SCF). Both the FLF and SCF methods are generalizations of the PRB method. The general block diagram of FLF [16] method is shown in Fig. 1.6. In this case, $t_i(s)$ can be first order low pass or high pass functions or alternatively second order biquadratic sections. The summation of the feedback

voltages is responsible for the realization of the poles of the function, while the second summation is required for the realization of any finite transmission zeros.

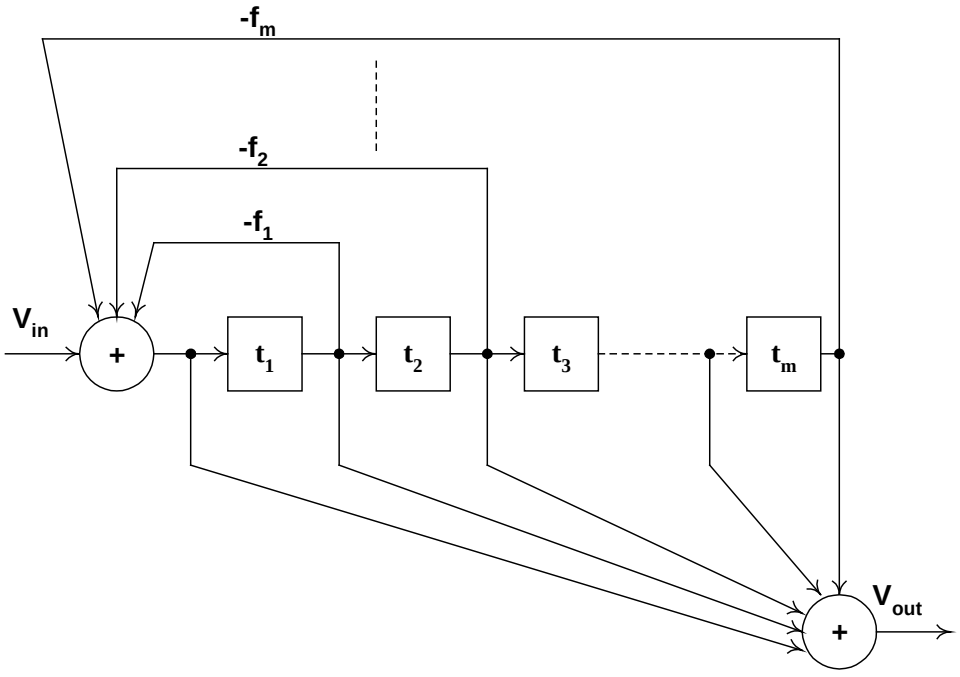

Fig. 1.6 Follow-the-leader feedback (FLF) topology

1.5.3 LC Ladder Simulation

Simulation of passive resistively terminated lossless ladder networks can be achieved by simulating either functionally or using active elements to implement the inductances of the ladder. Functional simulation [17] is implemented by realizing the currents and node voltages in the ladder. The LC ladder simulation method is attractive, because it leads to active filters of lower sensitivities the other two approaches, i.e., Cascade and MLF.

Table 1.2 summarizes different approaches to realize a high order filter.

Table 1.2 Approaches to realize a high order filter

Approach	Comments
Cascade	- Biquadratic sections are cascaded - Simple in designing and tuning the filter - Bad sensitivity performance
Multiple-loop feedback	- Multiple feedback is applied in cascade of biquadratic sections - Better sensitivity performance of the overall circuit
LC ladder simulation	- Simulation of passive lossless ladder networks - Best sensitivity performance

1.6. Automatic Tuning Schemes

Automatic tuning is of critical importance to control the frequency response of continuous-time filters. A tuning scheme is required in a continuous-time filter to compensate for the drift of element values due to process and temperature variations that will consequently affect the filter accuracy. Left on its own, the frequency response of an integrated filter can change by as much as 50% or more. The precision of the frequeny response of the filter, i.e., the center frequency, can be improved to a few percent, or even to a fraction of 1% by using automatic tuning techniques based on the master slave indirect tuning principle. This is implemented by means of a phase locked loop using either a voltage controlled filter (VCF), as shown in Fig. 1.7, or a voltage controlled oscillator (VCO), as shown in Fig. 1.8 [18].

In the first case, an external reference signal of well-controlled frequency $f_{external}$ is applied to the master filter which is similar to a second-order filter section which is similar to those used in the filter to be tuned. The frequency-dependent input-output phase characteristics of this reference are then exploited to tune the circuit. For this

reason, any offset in the phase comparator will result in a frequency tuning error. A rough calculation show that for a typical ±25% capture range (which is reasonable with respect to the variations in process variations), the quality factor of a second-order reference filter must be less than 2 [19]. From the corresponding phase response, and offset of 2^0 in the phase detection will result in a tuning error of about 1%. This puts stringent requirements on the phase comparator performance, i.e., accuracy and speed.

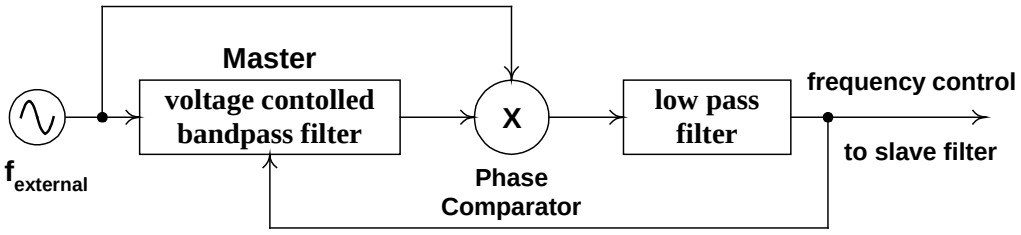

Fig. 1.7 Master-slave frequency tuning scheme based on a VCF

Another disadvantage of the VCF configuration is that harmonic distortion in the reference signal will introduce additional tuning errors. This is because the harmonics will not come out from the reference filter with the same phase shift as the fundamental frequency. When multiplied with the incoming signal, these residual out-of-phase harmonics will alter the result of phase comparison. Some of those distortions are dc components. This dc component can be considered as noise, which will produce error on the dc output of the phase comparator. Since this dc voltage is the control voltage of the slave filter, the harmonic distortion should be minimized. This can be achieved by using

a sinusoidal reference signal instead of a clock signal. An additional filter for the reference signal is needed in this case.

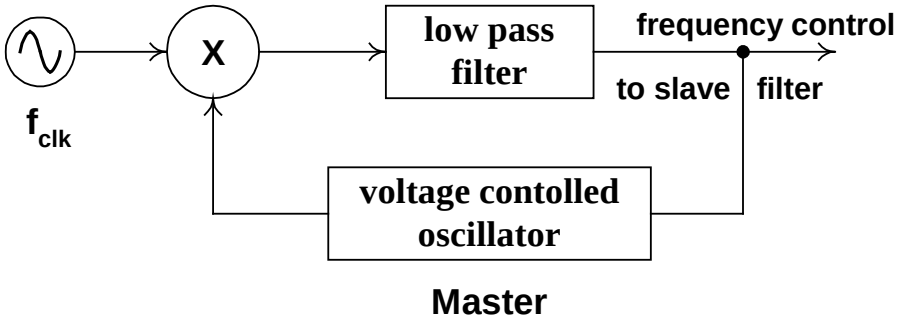

Fig. 1.8 Master-slave frequency tuning scheme based on a VCO

In the VCO approach, the multiplier or the phase comparator has to compare the frequency of the signal coming out from the VCO with that of the reference signal. The error voltage is filtered out by the low pass filter and fedback to the voltage-controlled oscillator. As opposed to the VCF approach, absolute phase accuracy is not necessary since only the phase variations, i.e., frequency, of one signal with respect to the other must be detected. The requirements on the phase comparator are thus relaxed, i.e., for example a simple XOR gate can be used. For the precision of the tuning system, the important parameter is the oscillating frequency of the VCO. Thus, this approach is less sensitive to the intermodulation effects and nonlinearities of the phase comparator.

The main problem then is the implementation of a voltage-controlled oscillator that is well matched to the filter to be tuned. The best candidate is usually a second-order harmonic oscillator, the amplitude regulation of which must be carefully considered

since harmonic distortion and nonlinearities in the transconductors would shift the effective oscillation frequency, thus introducing a tuning error. Thus the oscillation amplitude must be kept limited to the linear portion of the transconductors used by means of a limiter. Another design consideration of the VCO technique is the feedthrough from the oscillator to the filter, which should be minimized.

Master-slave techniques are ultimately limited by the mismatches of the main filter elements. This problem is more prominent in high frequency where the filter becomes more sensitive to parasitics which are extremenly difficult to match in the master and the slave. Another problem is that the reference signal is usually in the filter passband, for better matching, making it very possible to leak to the output of the slave especially at high frequency applications. This can be partially solved if the control loops are operating in the stopband of the filter. The previous two problems are conflicting. For better matching betwwen the master and the salve, it is desirable to layout them as close as possible. This makes the problem of noise feedthrough even worse, which may be even higher than the noise level of the filter itself.

Even with perfect matching, the precision of the tuning control loop itself is limited. Finite loop gain, excess phase errors, DC offsets, limitations of both multipliers and peak detectors are all contributing to the error in the tuning loop. Again all those nonidealities are more prominent at high frequency. Thus, the automatic tuning of filters operating at very high frequencies (RF range) is still a challenge and an open problem for investigation. Direct tuning can be applied to tune the filter that does the processing

itself to avoid some of the above problems. This can be done in idle time slots available in TDMA wireless standards [20].

For narrow-band filter applications the filter bandwidth must be also tuned. Several Q tuning schemes have been reported in the literature with a precision as good as 1% [21]. It is also worth mentioning that there is a possibility of interaction between the frequency tuning loop and the Q tuning loop. However, if one tuning loop (usually the Q loop) is made much slower than the other, the two loops can be considered practically decoupled. In [45] the order of the f_0 and Q tuning is not that critical.

A digital frequency tuning technique [22] is shown in Fig. 1.9. The tuning circuit consists of an oscillator, two counters, one up/down counter, and control logic. The number of bits of the up/down counter (number of digital programmable array in the filter/oscillator) determines the resolution of this tuning scheme. To achieve frequency tuning, the oscillator output is passed to a counter to measure the oscillator frequency. The other counter is used to to measure a reference frequency. The values stored in both counters are compared at the end of each calibration cycle. The control logic decides, according to the content of both counters, which direction to move the up/down counter. If the two values are equal, the tuning is freezed with the final digital frequency control value stored in the up/down counter.

In an OTA-C filter, frequency tuning can be achieved by tuning the transconductors using a control voltage or by tuning the capacitors using a programmable capacitor array (PCA). The first solution implies changing the dynamic range of the filter since the bias conditions of the OTA and thus linearity of the filter is changed. The second solution

using PCA is preferable to optimize the dynamic range of the filter during tuning at the expense of area since the PCA and associated switches require more area.

The conventional tuning circuit based on PLL, as discussed previously might not be suitable for filters with programmable capacitor arrays (PCAs). This is because the output of the filter in the PLL is an analog voltage, which cannot be interfaced directly with the PCAs. On the other hand, the digital frequency tuning scheme shown in Fig. 1.9 is very well suited with those type of applications where the frequency tuning is implemented using PCAs. The output of the counter is directly connected to the switches of the PCA without the need of an extra interface, i.e., an A/D converter.

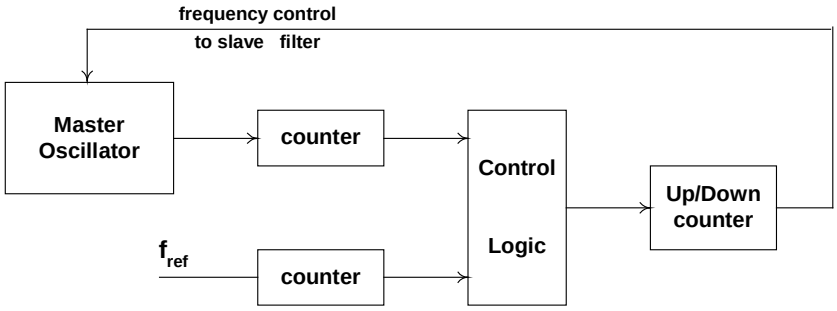

Fig 1.9 Schematic diagram for digital frequency tuning technique

1.7. Design Considerations

Some typical analog filter performance criteria are transfer function accuracy, linearity, noise performance, power consumption, and silicon area. Thus as the general case of analog design, the filter design entail multi-dimensional design trade-offs as shown in Fig. 1.10.

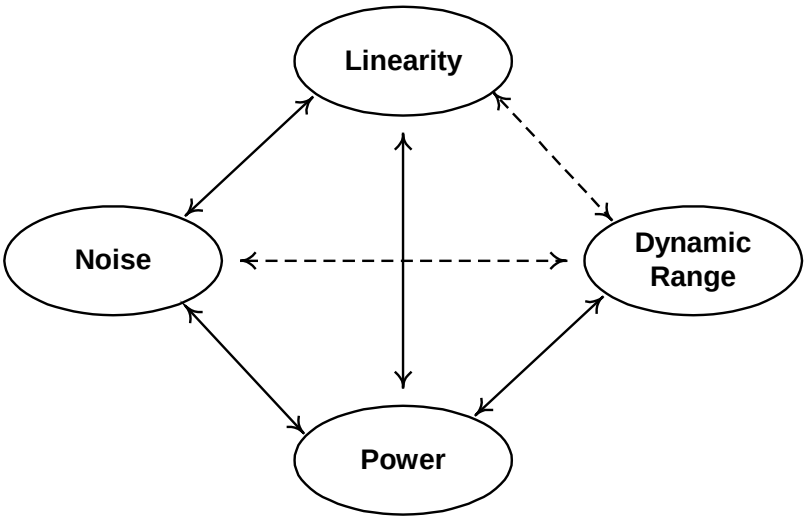

Fig. 1.10 Analog design trade-offs

What mainly limit the performance of an analog circuit are the non-idealities of the used building blocks and the circuit architecture. The research is concentrating on the design issues of high frequency continuous-time integrated filters. Some novel circuit building blocks are introduced such as the new OTA structure shown in Chapter II. Some novel circuit architectures are also presented such as the new 4^{th} order filter structure shown in Chapter IV. Discussion of different design considerations and trade-offs: high frequency, low voltage, power consumption, linearity, noise is left for each circuit separately as we advance through the thesis in the following chapters.

1.8. Organization

In each chapter of this dissertation an integrated circuit is presented. The application of the circuit and some background of what has been done previously in the literature are mentioned. The circuit is then introduced with the things and novel techniques that make

it different form what has been previously reported. The design considerations and the main limitations of the introduced techniques are also discussed. At the end of each chapter, the experimental results of the given circuit are shown.

The next three chapters presents three filters for three different applications. Chapter II proposes a new pseudo differential fully balanced fully symmetric CMOS OTA architecture with inherent common-mode detection. Through judicious arrangement, the common-mode feedback circuit can be economically implemented. The OTA is used to design a 100 MHz 4^{th} order OTA-C linear phase filter for hard disk drive read channel applications as shown in Fig. 1.11. The low pass filter (LPF) is needed to limit the noise bandwidth and provides anti-alias filtering prior to sampling the signal. The information content of the signal at the read head is the time at which pulses occur. Thus the group delay of the LPF needs to be constant in the frequency band where the spectral components of the signal are located. Otherwise it will be affecting the information content of the signal. Current state-of-the art read channel filters operate at 150 MHz or less [23-25]. OTA-C filters are one of the candidates of continuous-time filters suited for this application due to their suitability for high frequency operation.

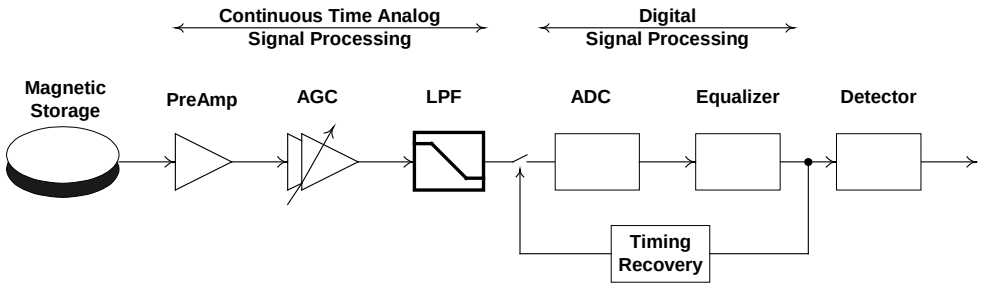

Fig. 1.11 Typical disk drive read channel

Chapter III presents a 5th order dual mode low-pass OTA-C filter. This filter is used as a low-pass channel selection filter, in a direct conversion receiver shown in Fig. 1.12, for two standards that have different bandwidths; Bluetooth and WLAN 802.11b.

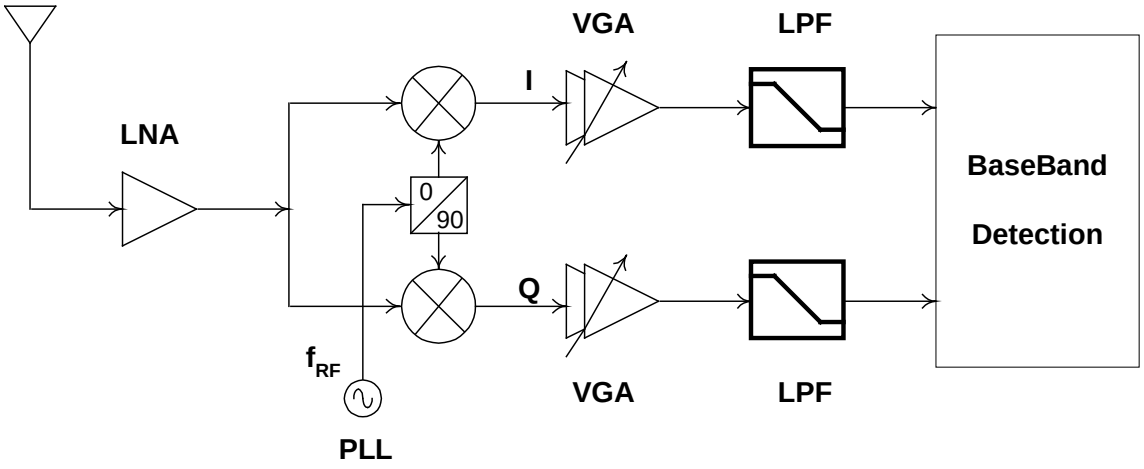

Fig. 1.12 Direct conversion receiver

The design is carried out in the IBM 0.25μm BiCMOS process and operates from 2.5V single voltage supply. The OTA used is based on a bipolar differential pair with source degeneration. The degeneration factor is kept constant in both standards by switching the degeneration resistors and the tail current source thus keeping linearity approximately the same for both standards. Frequency tunability is offered through capacitor banks.

Chapter IV introduces a low-voltage 4th order RF bandpass filter structure based on emulation of two magnetically coupled resonators that is intended to be replace the low noise amplifier (LNA) and the image rejection filter in a superheterodyne receiver. An example of a conventional super heterodyne receiver is shown in Fig. 1.13. The

architecture is not suitable for monolithic integration due to the usage of high frequency RF pre-select filter and high Q image rejection and channel select filters. Some attempts in literature have been made to combine the RF pre-select filter together with LNA [26-28] or the LNA together with the image rejection filter [29-31]. Few attempts have been made to replace the first three blocks before the first mixer with an LC filter that provides some bandpass gain [32].

A unique feature of the proposed architecture is using electric coupling to emulate the effect of the coupled-inductors, thus providing bandwidth tuning with small passband ripple. The filter has been implemented in HP 0.5μm CMOS process and works around 1.8GHz.

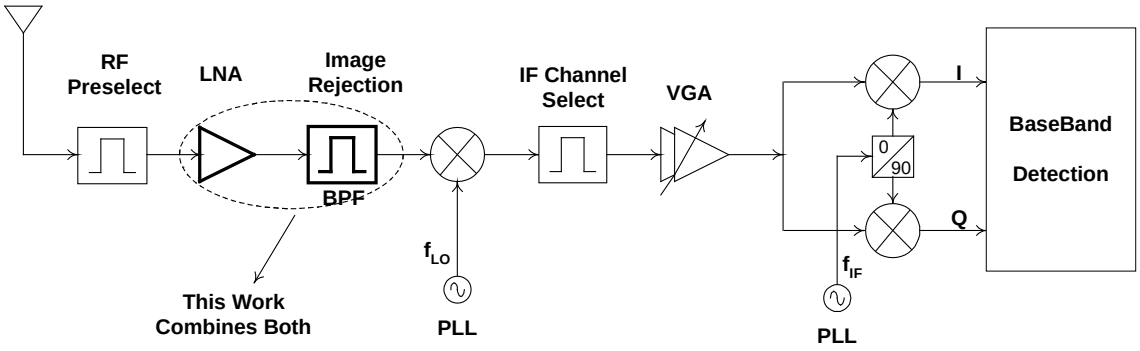

Fig. 1.13 Super heterodyne receiver

In chapter V, a low-power quadrature direct digital frequency synthesizer (DDFS) is presented. It is designed to be used in a Bluetooth transmitter as shown in Fig. 1.14. Since Bluetooth uses GFSK modulation scheme, a quadrature output DDFS can be used to generate the frequency-modulated signal.

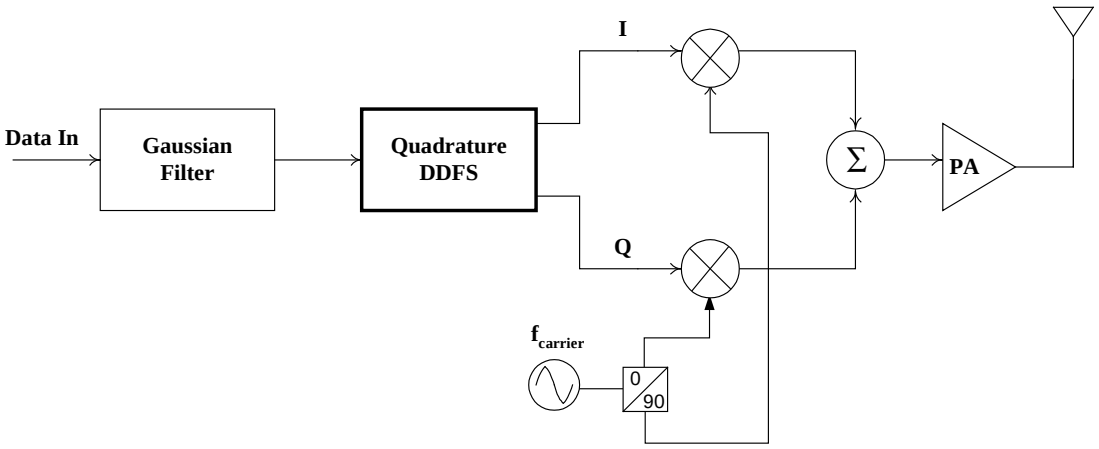

Fig. 1.14 Bluetooth transmitter architecture

Piecewise linear approximation is used to avoid using ROM look-up table to store the sine values in a conventional DDFS. Significant saving in power consumption, due to the elimination of the ROM, renders the design more suitable for portable wireless communication applications. To demonstrate the proposed technique, a quadrature DDFS has been implemented using 0.5μm CMOS process.

In Chapter VI, the implementation of an incremental A/D converter for a power supply voltage of ±1V is presented. The design relies on using floating gate technique in order to reduce the effect of nonlinear settling due to possible saturation of the input stage and to achieve good performance under low voltage operation. The converter has been implemented in 0.5μm CMOS technology with V_{TN}=0.65V and V_{TP}=-0.90V.

Finally, Chapter VII summarizes the main contributions of this research work.

CHAPTER II

A LOW-VOLTAGE FULLY BALANCED OTA WITH COMMON-MODE FEEDFORWARD AND INHERENT COMMON-MODE FEEDBACK DETECTOR *

2.1. Motivation and Background

In general, a fully differential structure has an improved dynamic range over its single ended counterpart. This is due to the properties of any differential structure, namely, better common-mode noise rejection, better distortion performance, and increased output voltage swing. An important disadvantage of a fully differential structure is the need of an extra common-mode feedback (CMFB) circuit; the reasons are twofold:

(1) To fix the common-mode voltage (V_{CM}) at different high impedance nodes that are not stabilized by the negative differential feedback; V_{CM} is usually chosen as a dc reference voltage (V_{REF}) yielding maximum differential voltage gain and maximum output voltage swing.

(2) To suppress the common-mode signal components on the whole band of differential operation that tend to saturate different stages.

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* Part of this chapter is reprinted with permission from "A Low-Voltage Fully Balanced OTA with Common Mode Feedforward and Inherent Common Mode Feedback Detector," by Ahmed N. Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, April 2003. *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 663-668.

In some cases and due to the system configuration, the CMFB requirements can be relaxed. For instance, if the common-mode gain is sufficiently small, as would be the case of a conventional differential pair based OTA with a tail current, the CMFB bandwidth might be reduced [33]. Its primary function will be to set the common-mode voltage and it should not consume much power. Nevertheless, for good power supply rejection, a wide bandwidth CMFB is needed. In other cases, when the OTA outputs are loaded by low impedances, the dc output voltages are well defined and assuming that the common-mode gain is small enough, there may be no need for the CMFB circuitry as would be the case of filters built using lossy integrators [34].

In this chapter, a practical pseudo differential OTA is proposed [35-36]. It is shown that a separate CMFB circuit can be avoided with appropriate arrangement of cascaded pseudo differential OTAs, for example in a filter. This approach takes advantage of the OTAs used for the differential-mode operation to render low common-mode gain without extra circuitry. The proposed OTA has inherently the common-mode detector; hence the CMFB is economically implemented. A general description of nonlinearities in pseudo-differential CMOS OTAs is presented [37]. This includes transistor mismatches, cross product of differential and common-mode signals, short channel effects, and nonlinear interaction between the common-mode detector used in the CMFB circuit and the differential signal. The proposed OTA is used as a case study to probe the theory.

2.1.1 Linearization Techniques

OTA-C filters based on transconductors working in open loop have the potential to operate at high frequencies, relative to the Active-RC filters based on OpAmp working in closed loop. However, the linear signal range of a transconductor is usually limited, also due to the open loop operation, which will consequently limit the dynamic range.

Linearization techniques [38] have been developed to make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent. In general, the drawbacks of linearization techniques are degradation of the frequency response of the OTA especially if many additional nodes are introduced, and the deterioration of the noise performance of the OTA especially if many additional devices are introduced. This is translated to payments in terms of higher power consumption and additional silicon area. It is very desirable that those drawbacks are minimized to get a net benefit from the linearization technique.

For a conventional differential pair with tail current source, a third order harmonic distortion, given by equation (2.1), does exist even assuming matching between the input transistors and a quadratic I-V characteristics of a transistor neglecting all short channel effects. See derivation of HD_3 in Appendix A.

$$HD_3 = \frac{v_d^{\,2}}{32(V_{GS} - V_T)^2} \tag{2.1}$$

2.1.1.1 Source Degeneration

One of the most natural high-frequency linearization techniques often used is source degeneration, shown in Fig. 2.1. It can be shown that the small-signal transconductance

is reduced by the factor $(1+g_mR)$ where g_m is the transconductance of transistors M_1 and $n=g_mR$ is the source degeneration factor. On the other hand, the third harmonic distortion improves relative to the case of a simple differential pair, as given in equation (2.2), by the factor $(1+n)^2$.

$$HD_3 = \frac{v_d^{\,2}}{32(1+n)^2(V_{GS}-V_T)^2} \tag{2.2a}$$

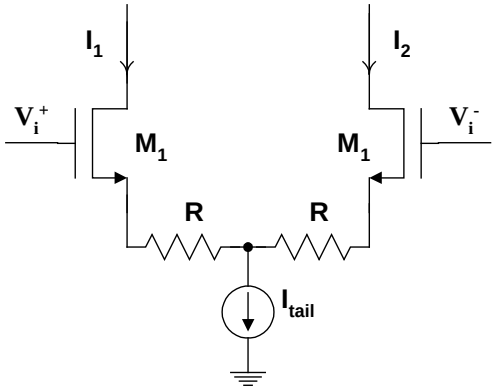


Fig. 2.1 Linearization using source degeneration

2.1.1.2 Attenuation

Another category of linearization techniques is attenuation. In this category, the input voltage is attenuated by a factor m, i.e., $V_{in,att}=mV_{in}$. This will result in reducing the transconductance by the same factor, i.e., $g_{m,att}=mg_m$, and improving the linearity by the factor m^2. For an attenuation factor m, and using equation (2.1), the third order harmonic distortion can be derived as:

$$HD_3 = \frac{v_d^{\,2}}{32m^2(V_{GS}-V_T)^2} \tag{2.2b}$$

There are many techniques in this category. One approach is to use a series of differential pairs, as shown in Fig. 2.2. This effectively split the voltage in the sections by m where m is the by the number of sections used. The major drawback of this approach is the degradation of the phase response with increasing the number of sections. For the case of two sections, the attenuation factor m is 2 and using equation (2.2b), HD_3 of Fig. 2.2 can be written as:

$$HD_3 = \frac{v_d^{\,2}}{128(V_{GS} - V_T)^2} \tag{2.2c}$$

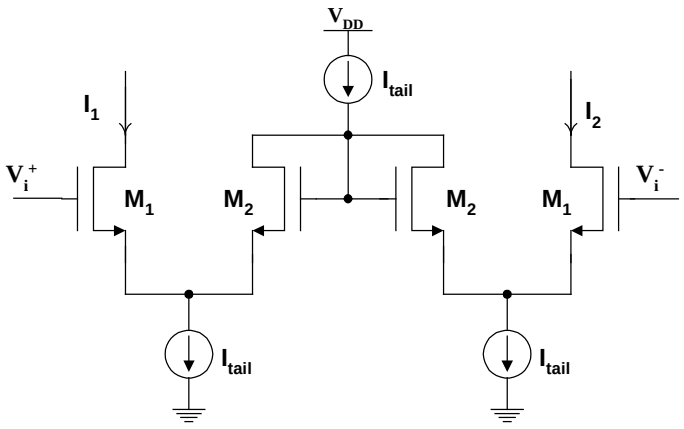


Fig. 2.2 Linearization using series of differential pairs

Another approach in this category is the use of floating gates, as shown in Fig. 2.3. Floating gates provide a natural capacitive divider for the input signal. Thus, the effective input ac voltage applied to the floating gate (FG) is reduced by the factor $k=(C_2+C_1)/C_1$, where C_1 and C_2 are the capacitances associated with the input signal and the bias voltage, respectively. Although floating gate techniques are very attractive for low voltage applications [39]; their usage in high frequency is limited due to the

capacitive coupling elements involved. The noise performance of the floating gate transistor is also deteriorated with respect to its conventional counterpart. The output refereed noise is the same, but the input refereed noise is increased by the factor k^2.

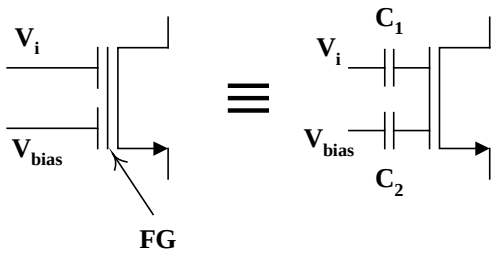


Fig. 2.3 Linearization using floating gates

A third approach in the attenuation category is using bulk driven transistors, as shown in Fig. 2.4. The transconductance of a transistor driven from the bulk rather than the gate is reduced by a factor γ, where γ is in the range of 0.2 and 0.4 and depends very much on the technology used. Bulk-driven technique is also attractive for low voltage applications [40] but it suffers from worse frequency response, with respect to the conventional gate drive case. The equivalent noise and area of a bulk driven transistor is also larger than a conventional gate drive transistor. It also suffers form potential latch up problems.

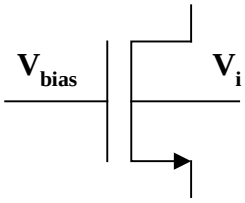


Fig. 2.4 Linearization using bulk driven transistor

Attenuation factors of different techniques are shown in table 2.1. It is obvious in all of the attenuation techniques mentioned above that the transconductance is reduced by the attenuation factor and hence need to be compensated at the expense of power consumption and/or silicon area. Note that more than one linearization technique can be combined together to achieve better linearity [38].

Table 2.1 Attenuation factors of different techniques

Attenuation technique	**Attenuation factor (m)**
Series of differential pairs	number of sections used
Floating gate	$(C_2+C_1)/C_1$
Bulk driven	$2.5 < (1/\gamma) < 5$

2.1.2 CMFB Design Considerations

A CMFB circuit is classically performed by means of an additional loop as shown in Fig. 2.5. The output common-mode level (V_{CM}) is sensed using a common-mode detector, i.e., $V_{CM} = (v_{OUT}^{+} + v_{OUT}^{-})/2$. It is then compared with the reference voltage $V_{REF,}$ and an error-correcting signal is injected to the biasing circuitry of the OTA. The CMFB loop has to be designed carefully to avoid potential stability problems. This increases the complexity of the design, the power consumption, and the silicon area used. The frequency response of the differential path is often affected due to the added parasitic components involved in conventional CMFB schemes.

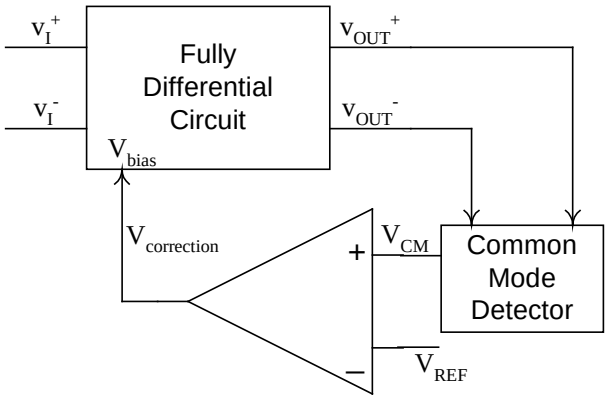


Fig. 2.5 Conventional CMFB loop

An important design consideration for a CMFB loop is to have has few parasitic poles to be able to compensate the common-mode loop without severely limit its bandwidth, or equivalently its speed. The high speed of the CMFB loop is essential to reject high-frequency common-mode noise that can otherwise saturate the outputs. It is critical when designing a CMFB circuit to check the step response (or transient response) of the CMFB loop, as discussed in section 2.4.2, and verify that enough phase margin exists.

Another design consideration for a CMFB circuit is linearity. Since the CM detector is nonlinear, it will degrade the distortion performance of the differential path. The nonlinear interaction between the differential-mode and common-mode loops results in second and third order harmonic distortions at the differential output signal [41], as will be shown in section 2.3. Thus, a suitable common-mode signal detector should be chosen carefully to reduce the impact of its nonlinearity on the differential components.

Some of the most commonly used common-mode detectors and their characteristics are shown in Table 2.2 [42]. The performance of CM detector is specified by its nonidealities. In general, the small-signal output V_{CM} of a CM detector can be written as:

$$V_{CM} = \alpha_1 V_{o,CM} + \alpha_2 V_{o,DM} + \alpha_3 V_{o,DM}^2 \tag{2.3}$$

The first term would be the only output if the CM detector is ideal, the second term arises due to mismatches, and the third term is due to nonlinearities.

Table 2.2 Common-mode detectors and their characteristics

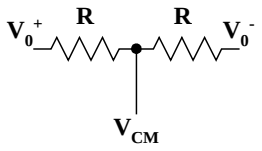
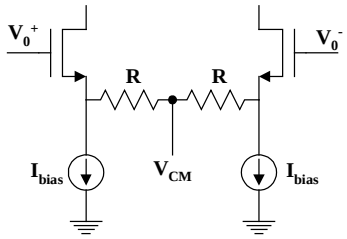
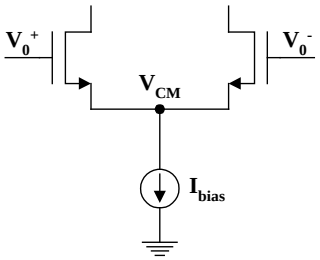
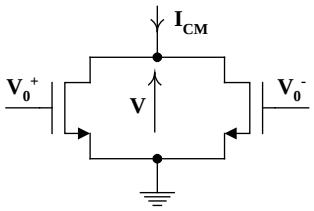
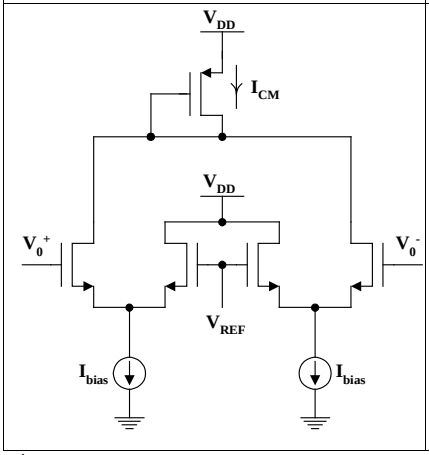
Common-mode detector	**Characteristics**	**Performance***
	- Excellent linearity - Suitable only for OpAmp with low output impedance - A buffer is needed for an OTA with high output impedance	$\alpha_1=1$ $\alpha_2=(\Delta R/4R)$ $\alpha_3=0$
	- High dc offset due to source followers - Second order harmonic distortion is dominated by mismatches in the resistors. - Limited common-mode range - See Fig. 3.10 & Fig. 3.11	$\alpha_1=1$ α_2^+ $\alpha_3=(1/2I_B)(1/\sqrt{8\beta I_B})$ $(1/2R+\sqrt{2/\beta I_B})^2$
	- Highly nonlinear - High dc offset	$\alpha_1=1$ $\alpha_2=(\Delta\beta/4\beta)$ $+(\Delta V_T/4)\sqrt{\beta/I_B}$ $\alpha_3\cong 0$

Table 2.2 (continued)

Common-mode detector	Characteristics	Performance*
	- Transistors operate in the linear region - Third order harmonic distortion dominated by mobility degradation	$\alpha_1=2\beta\Delta V$ $\alpha_2=0.5\Delta\beta\Delta V$ $\alpha_3=0$
	- Good transconductance - Excellent linearity	$\alpha_1=\sqrt{\beta I_B+(\beta\Delta V_T/4)+}\ (\Delta\beta/2)$ $\sqrt{(I_B/\beta)}$ $\alpha_2\cong(\Delta I_B/8)\ \sqrt{(\beta/\ I_B)}$ $\alpha_3\cong0$

* β is the transconductance parameter, V_T is the threshold voltage

+ $\alpha_2=(\Delta R/4R)+(1/\sqrt{\ 8\beta I_B})[\Delta R/2R+\Delta I_B/4I_B+\Delta\beta/4\beta/(2R+\sqrt{\ 2/\beta I_B})]+(1/\sqrt{\ 8\beta I_B})[\Delta V_T+(\Delta I_B/4I_B)\sqrt{(I_B/\beta)}/(2R+\sqrt{\ 2/\beta I_B})^2]$

The third design consideration for a CMFB circuit is suitability for low voltage. In some cases, the amplifier might be capable of working at low voltage and the bottleneck becomes the design of an appropriate common-mode detector working with the same low voltage without sacrificing its linearity performance. The design of CMFB circuits that are linear and can operate from low voltage is an area of active research.

This chapter is organized as follows: Section 2.2 shows the proposed OTA and discusses its properties and advantages. The general description of nonlinear effects in a pseudo-differential OTA with CMFB is presented in section 2.3. Section 2.4 discusses

the CMFB loop considerations. An example of the use of the OTA in a linear phase filter is shown in section 2.5. The experimental results are shown in section 2.6. Finally, concluding remarks are drawn in section 2.7.

2.2. Proposed OTA Architecture

In general, operational transconductance amplifiers can be divided into two main groups: Fully Differential (FD) and Pseudo Differential (PD). FD is typically based on a differential pair with tail current source and PD is based on two independent inverters without tail current source as shown in Fig. 2.6(a). Avoiding the voltage drop across the tail current source, in a PD structure, allows achieving wider input range and makes the architecture attractive for low voltage applications. Removing the tail current source, however, results in larger common-mode gain (A_{CM}).

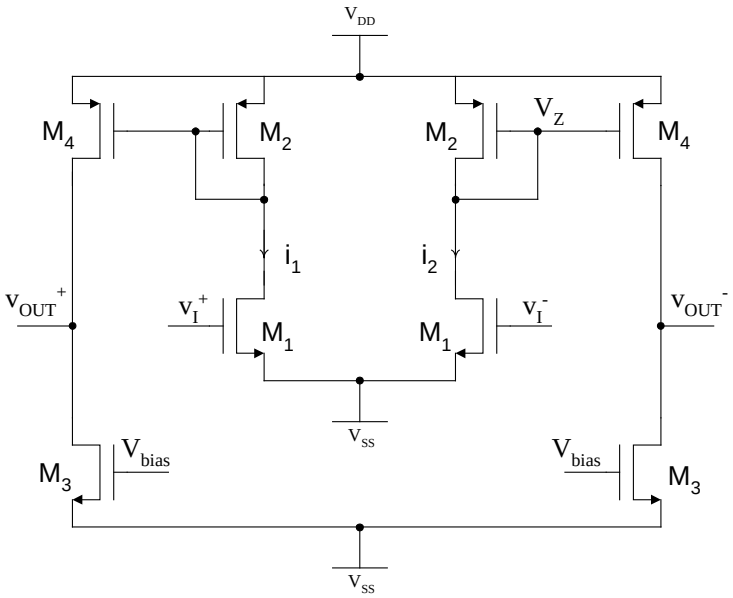


Fig. 2.6(a) Conventional pseudo differential OTA

In a FD structure, the common-mode gain can be reduced by increasing the output impedance of the tail current source. However, for the PD OTA shown in Fig. 2.6(a), A_{CM} is equal to the differential-mode gain $A_{DM}(=g_m.r_0)$, i.e., $CMRR=A_{DM}/A_{CM}=1$. This large A_{CM}, in PD structures, can lead to huge common-mode variations at the OTA outputs unless a fast and strong CMFB is used.

Using a balanced configuration with two single-ended transconductances [33], as shown in Fig. 2.6(b), reduces A_{CM} at low frequency to the order of unity as given by:

$$A_{CM}\big|_{\omega=0} = \frac{v_{ocm}}{v_{icm}}\bigg|_{\omega=0} = \frac{g_{m1} - \dfrac{g_{m1}.g_{m2}}{g_{m2}+g_{01}+g_{02}}}{g_{01}+g_{02}} = \frac{g_{m1}}{(g_{m2}+g_{01}+g_{02})} \cong \frac{g_{m1}}{g_{m2}} \qquad (2.4)$$

Observe in the first part of (2.4) that due to the finite output conductance of the OTA, A_{CM} is finite (non-zero) [43]. The previous approach adds more load to the driving stage due to the connection of two input transistors, thus doubling the input capacitance.

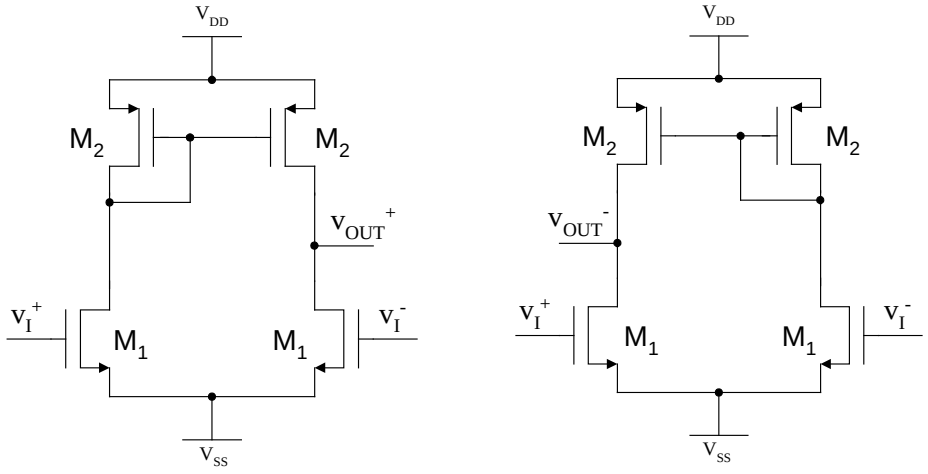


Fig. 2.6(b) Balanced configuration with two single-ended OTAs

A pseudo-differential OTA with common-mode feedforward (CMFF) reported in [44] uses a separate BiCMOS transconductance for common-mode detection. The pseudo differential OTA with CMFF reported in [44] uses a separate transconductance for common-mode detection. This approach adds more load to the driving stage due to the connection of two input transistors, one for the differential transconductance and the other for the common-mode transconductance as shown in Fig. 2.6(c), thus doubling the input capacitance[1]. A CMOS pseudo-differential version [45] is shown in Fig. 2.6(d).

Although CMFF improves the rejection to common-mode signals, it is incapable to fix properly the dc common-mode output voltage. It needs to be fixed by the means of an additional CMFB circuit. Without loss of generality, the CMFB for a pseudo-differential OTA can be implemented as shown in Fig. 2.7. How to implement Fig. 2.7 in an efficient way is also discussed in the following sections.

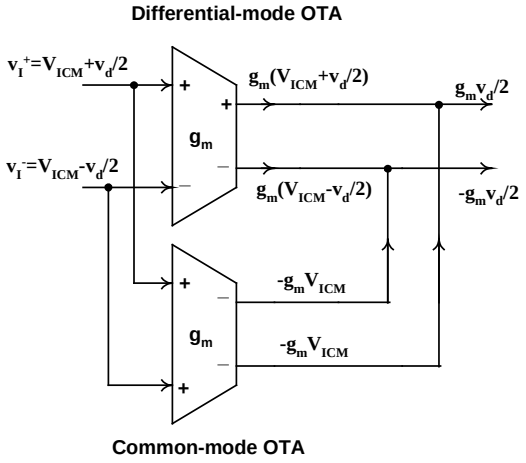


Fig. 2.6(c) Pseudo-differential OTA with CMFF [Conceptual structure]

[1] Also Miller effect (of the C_{gd} capacitors of M_1) degrades the frequency response

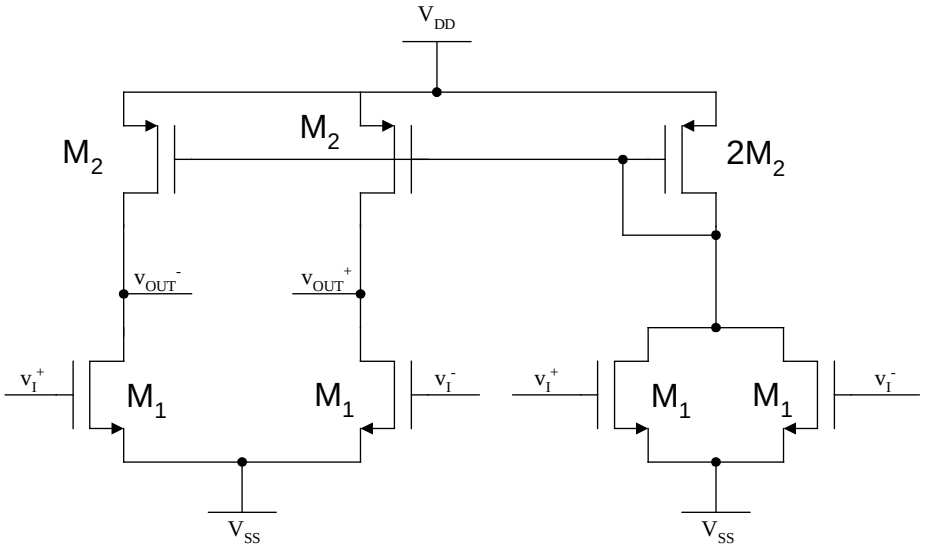


Fig. 2.6(d) Pseudo-differential OTA with CMFF [Circuit implementation]

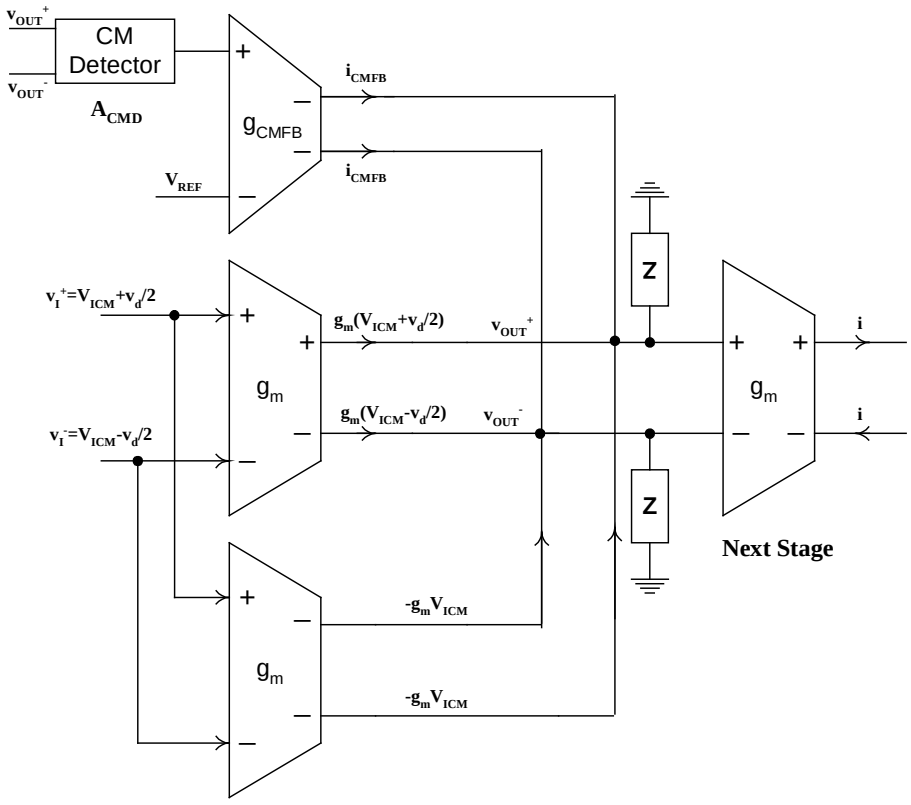


Fig. 2.7 Pseudo-differential OTA with CMFF and CMFB

The conceptual idea and the circuit implementation of the proposed fully symmetric fully balanced OTA are shown in Fig. 2.8(a) and Fig. 2.8(b) respectively. The common-mode detection is done using the same differential transconductance by making copies of the individual currents and subtracting the common-mode current at the output. It has four current mirrors, no tail current source. The proposed OTA can be described as a conventional three current mirror single ended OTA, without the tail current, plus the additional branches (dashed lines). Thus, the OTA becomes fully balanced [46] and fully symmetric with enhanced features, to be described in the next sections.

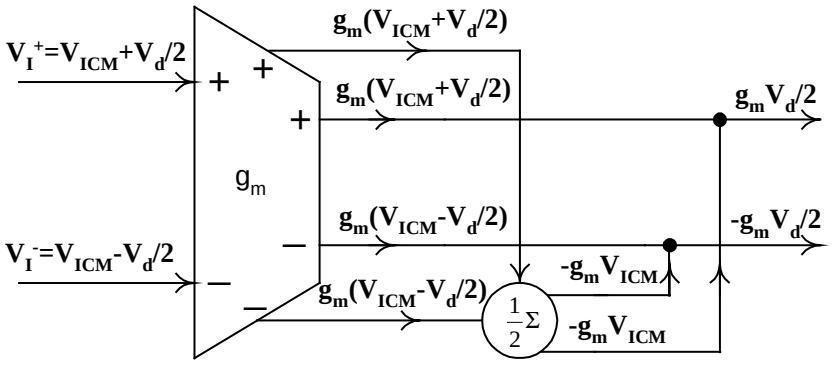


Fig. 2.8(a) Conceptual structure of the proposed OTA architecure with CMFF

2.2.1 Inherent Common-Mode Detection

Transistors M_3 and M_4 [bold in Fig. 2.8(b)] provides the information of the common-mode level of the inputs $V_{ICM} = (v_I^+ + v_I^-)/2$; it can be easily shown that if short channel effects are not considered, then:

$$i_1 + i_2 = 2.\frac{K_P}{2}\left(\frac{W}{L}\right)_1\left[\left(V_{DD} - V_{ICM} - |V_{TP}|\right)^2 + \frac{v_d^2}{4}\right] = \beta\left[V_{ov}^2 + \frac{v_d^2}{4}\right] = \beta.V_{ov}^2 - 2\alpha_3.v_d^2 \qquad (2.5)$$

where $v_I^+ = V_{ICM} + v_d/2$, $v_I^- = V_{ICM} - v_d/2$, $\beta = K_P(W/L)_1$, $\alpha_3 = -\beta/8$, and $V_{ov} = V_{DD} - V_{ICM} - |V_{TP}|$ is the overdrive voltage. Note that $(i_1+i_2)/2$ is being mirrored to the output yielding the desired extraction of the common-mode information V_{ICM}.

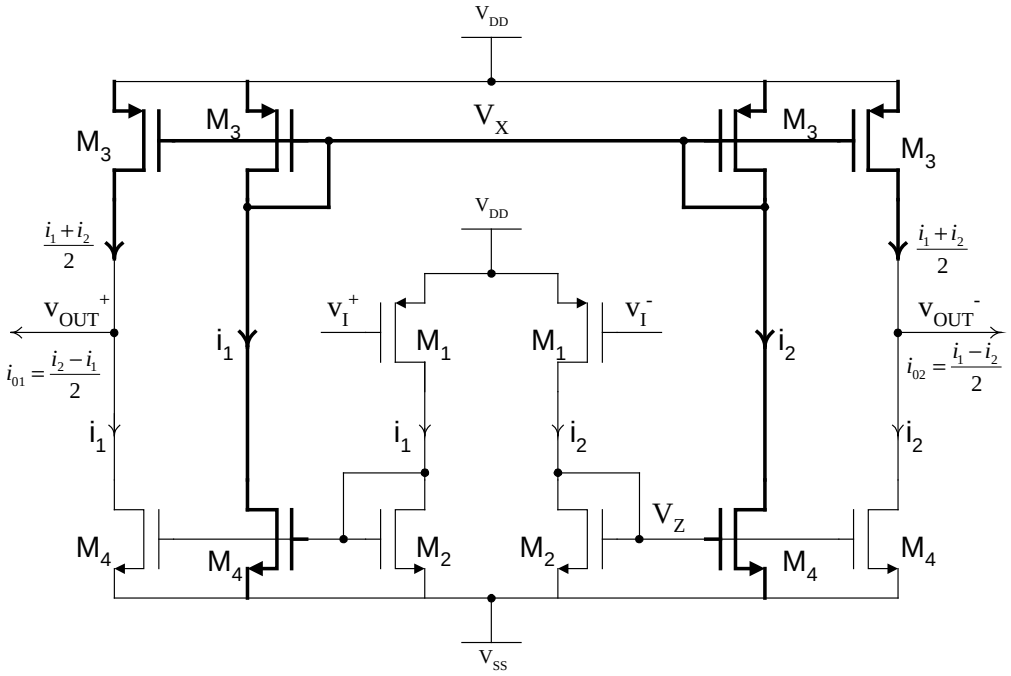


Fig. 2.8(b) OTA architecure with CMFF (M_4=BM_2)

2.2.2 Inherent Common-Mode Feedforward

In Fig. 2.8(b), the common-mode current $(i_1 + i_2)/2$ is subtracted at the OTA output nodes; hence a feedforward cancellation of the common-mode input signal is performed, yielding (for M_4=BM_2):

$$i_{01} = \frac{i_2 - i_1}{2} = B\frac{K_P}{2}\left(\frac{W}{L}\right)_1 \left[V_{DD} - V_{ICM} - |V_{TP}|\right] v_d \,,\; i_{02} = -i_{01} \tag{2.6a}$$

$$i_{od} = i_{01} - i_{02} = i_2 - i_1 = B \times \beta \times V_{ov} \times v_d = g_m v_d \tag{2.6b}$$

2.2.3 CMFB and CMFF Arrangements

Although the CMFF provides rejection to the common-mode components at the output, we still need to fix the dc common-mode output voltage. This is traditionally done using an additional CMFB circuit [see Fig. 2.5]. In the proposed OTA architecture, there is no need to add a separate common-mode detector to implement the CMFB circuit. In fact, the same effect (CMFB) can be obtained by judiciously connecting at least two of the proposed OTAs. The common-mode information obtained at node V_X can be used in a CMFB arrangement [47], as shown in Fig. 2.8(c). The connection at the output stage is taken from V_X of the next stage, which is now sensing the common-mode level of the output (input of the next stage).

To take full advantage of feedback and feedforward properties, both techniques (CMFB and CMFF) can be combined by adding the four transistors $\overline{M}_3$ and $\overline{M}_4$, as shown in Fig. 2.9. The signal common-mode components are suppressed by the action of the CMFF. The dc level of the output is sensed by the input of second stage, and the common-mode level is detected at node V_X (drain current of $\overline{M}_3$). It is then compared to the required reference (drain current of $\overline{M}_4$), fixing the dc output level to the required value (zero in our particular case). The requirement of the additional implementation of the CM voltage detector used in conventional CMFB schemes is eliminated.

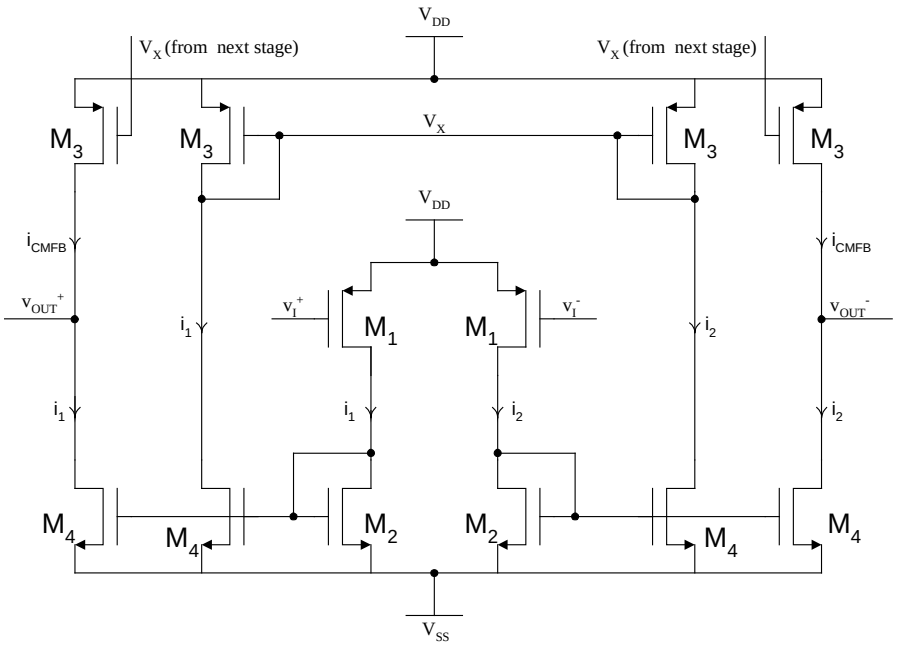


Fig. 2.8(c) OTA architecture with CMFB arrangement (M_4=BM_2)

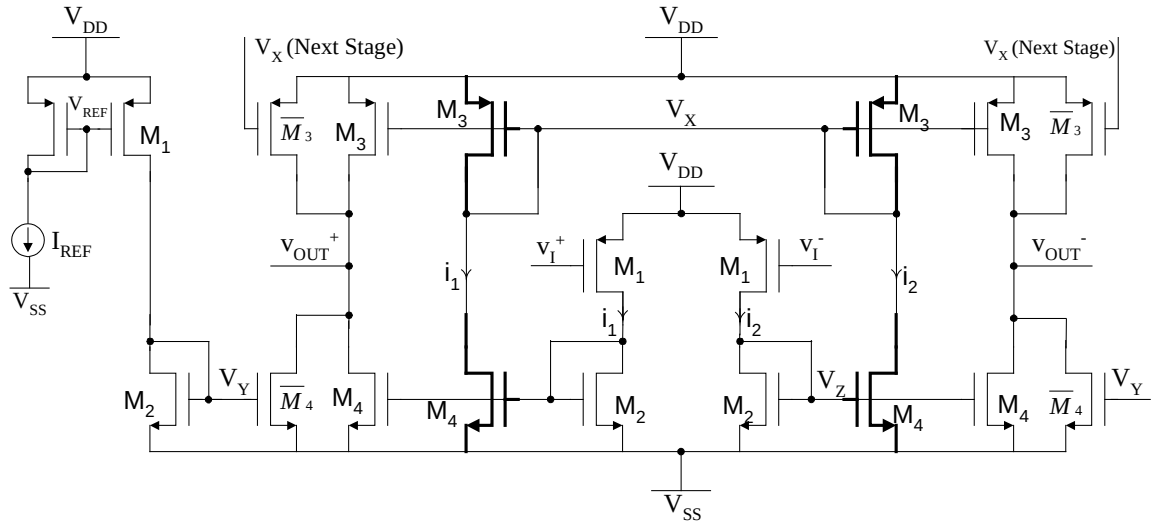


Fig. 2.9 Proposed OTA with CMFF and CMFB

In addition, this arrangement has the advantage that differential-mode signals and common-mode signals share basically the same loop if grounded capacitors are used,

and the low frequency transconductance of the CMFB loop is the same as the differential transconductance. Thus, it becomes easier to achieve similar bandwidth for common-mode and differential-mode loops.

2.2.4 Frequency Response and Excess Phase

For the OTA architecture in Fig. 2.8(b) there is only one path for the differential signal to the ouput which encounters one pole. The other path is a common-mode path. Thus, it can be expected that the OTA will have a single pole, and consequently small excess phase. The same applies to the proposed OTA in Fig. 2.9. Hence, the differential-mode transconductance can be approximated as (for M_4=M_2, i.e., B=1):

$$g_m(s) = \frac{i_{od}}{v_d} \cong g_{m1} \frac{g_{m2}}{g_{m2} + sC_Z} = \frac{g_{m1}}{1 + s/\omega_{nd1}} \tag{2.7a}$$

$$A_{DM}(s) = \frac{v_{od}}{v_d}(s) = \frac{g_{m1} g_{m2}}{(g_{m2} + sC_Z)(g_0 + sC_L)} \tag{2.7b}$$

where C_Z is the total parasitic capacitance ($\cong C_{gs2}+2C_{gs4}$) at node V_Z, C_L is the load capacitance, and g_0 is the overall OTA output conductance. Assuming $C_{gs2} \cong C_{gs4}$, the non-dominant pole ω_{nd1} is given by:

$$\omega_{nd1} = \frac{g_{m2}}{C_Z} \cong \frac{\sqrt{2\mu_n C_{ox}(W_2/L_2) I_{DC}}}{3\times 2/3 \times C_{ox} W_2 L_2} \cong \frac{\sqrt{2\mu_n C_{ox} I_{DC}}}{2.C_{ox} W_2^{1/2} L_2^{3/2}} \tag{2.8}$$

The excess phase $\Delta\phi$ can be expressed as:

$$\Delta\phi = -\tan^{-1}(\omega/\omega_{nd1})\Big|_{\omega << \omega_{nd1}} \cong -\omega/\omega_{nd1} \cong -\omega \frac{\sqrt{2C_{ox}}.W_2^{1/2} L_2^{3/2}}{\sqrt{\mu_n I_{DC}}} \tag{2.9}$$

Note that $\Delta\phi$ is miminized if the gate area is minimized as well.

Although the CMFF scheme of Fig. 2.8(b) creates a non-dominant pole, it is still more suitable for high frequency applications than the CMFF scheme of Fig. 2.6(d); it is true in principle that the parasitic capacitors can be absorbed in the integrating capacitors of the filter. Nevertheless, it is extremely difficult to do so in high frequency applications, where using large transconductances and small integrating capacitors is a must. In the CMFF scheme of Fig. 2.6(d), the parasitic capacitors contribute a large percentage of the total integrating capacitor making it difficult to control properly the filter cut-off frequency. On the other hand, the non-dominant pole in the proposed scheme can be pushed to high frequency by designing the current mirrors accordingly, for instance, choosing minimum length for transistors M_2. There are trade-offs between dc voltage gain, excess phase and current mirror accuracy.

2.2.5 Noise Performance

The bold transistors in Fig. 2.9 contribute to common-mode noise only due to the symmetric configuration, and thus their effect can be neglected. Adding the noise contribution of other transistors, the input referred noise density yields (for $\overline{M}_3$=M_3 and $\overline{M}_4$=M_4):

$$V_{in,\,n\_rms}^2 = 2.V_{n\_M1}^2 + \frac{2\times V_{n\_M2}^2}{(g_{m1}/g_{m2})^2} + \frac{4\times V_{n\_M3}^2}{(Bg_{m1}/g_{m3})^2} + \frac{4\times V_{n\_M4}^2}{(Bg_{m1}/g_{m4})^2} \qquad (2.10a)$$

Consider only the integrated thermal noise power, where $V_{n\_M}^2 = (8KT/3g_m).BW$, the input referred noise becomes:

$$V_{in,n\_rms}^2 = \frac{16KT}{3g_{m1}}.BW.\left[1+\frac{g_{m2}}{g_{m1}}+\frac{2g_{m3}}{g_{m1}B^2}+\frac{2g_{m4}}{g_{m1}B^2}\right] \quad (2.10b)$$

where BW is the equivalent noise bandwidth.

Increasing B will reduce the noise contribution of the output transistors, increase the effective transconductance and consequently g_{CMFB}, but it directly deteriorates the excess phase as C_Z increases. The accuracy of the current mirror is smaller for large values of B. In this design B is chosen to be unity to maintain the ability for high frequency operation. Increasing g_{m1} will also reduce the noise at the expense of larger power consumption.

2.3. Nonlinearity Analysis

The linearization of the output current in a PD OTA relies on the cancellation of the quadratic components of the individual currents [i_1 and i_2 in Fig. 2.6(a)].

$$i_1 = \frac{K_N}{2}\left(\frac{W}{L}\right)_1\left[v_I^+ - V_{SS} - V_{TN}\right]^2 = \frac{\beta}{2}\left(V_{ov}^2 + v_d V_{ov} + \frac{v_d^2}{4}\right) \quad (2.11a)$$

$$i_2 = \frac{K_N}{2}\left(\frac{W}{L}\right)_1\left[v_I^- - V_{SS} - V_{TN}\right]^2 = \frac{\beta}{2}\left(V_{ov}^2 - v_d V_{ov} + \frac{v_d^2}{4}\right) \quad (2.11b)$$

$$i_o = i_1 - i_2 = \beta V_{ov} v_d = g_m v_d \quad (2.11c)$$

Note that to a first-order approximation, the PD OTA is linear in contrast with a FD OTA. In the following sections, a general description of nonlinearities due to higher-order effects in pseudo-differential OTAs is discussed.

2.3.1 Transistor Mismatches

Due to transistor mismatches, the nonlinearity cancellation is not perfect and second-order harmonic distortion components will result at the differential output signal. Assuming a mismatch factor ε in the dimensions of the input driver transistors M_1 results in a second harmonic distortion (HD_2) in the output current i_o, obtained by replacing β by β(1+ε) in (2.11), given by (for $v_d = V_{Peak}\cos\omega t$):

$$HD_2 = \frac{\varepsilon}{8}\frac{V_{Peak}}{V_{ov}} \tag{2.12}$$

Fig. 2.10(a) shows the effect of mismatch of the input driver transistors M_1 on HD_2 of the OTA shown in Fig. 2.8(b). The differential input signal is fixed to $1V_{pp}$. The third harmonic distortion HD_3 (due to short channel effects as discussed in section 2.3.3) is fairly constant and it is the dominant source of distortion up to about 4% of mismatch; this is mainly due to inherent even-order harmonic distortion cancellation of the CMFF technique. HD_2 contributes to the THD almost the same as HD_3 at 4.5% of mismatch.

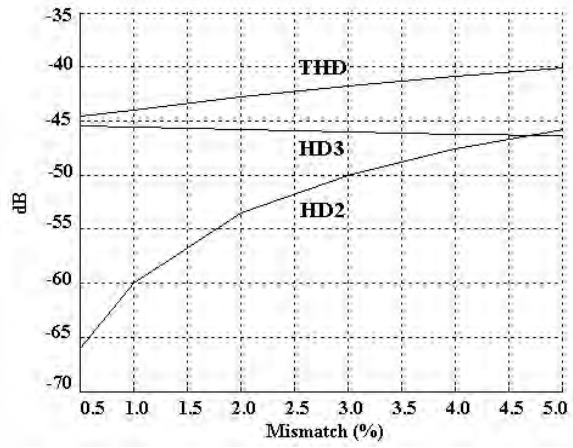


Fig. 2.10(a) Effect of transistor mismatches; v_d=1V_{PP} V_{DD}=1.65V, V_{SS}=1.65V

Fig. 2.10(b) shows the simulated HD_2, HD_3, and THD results of the OTA using BSIM models available through MOSIS while introducing 2% transistor mismatch. The THD is less than -40dB for differential input signals of amplitudes up to $1.2V_{pp}$, while operating from ±1.65V power supplies.

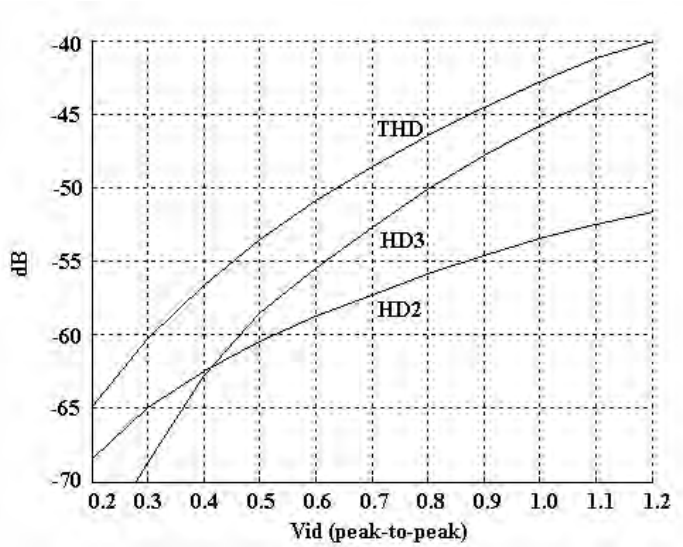


Fig. 2.10(b) HD_2, HD_3 and THD with 2% transistor mismatches

2.3.2 Cross product of differential and common-mode input signals

Additional harmonic distortion components can also appear, even neglecting all mismatches, due to the cross product of differential and common-mode input signals; hence the common-mode signals have to be suppressed as much as possible as well [35]. Let us assume a common-mode input interferer v_{cm} in addition to the differential-mode input signal v_d, then we can write:

$$i_1 = \frac{K_N}{2}\left(\frac{W}{L}\right)_1\left[v_I^+ - V_{SS} - V_{TN}\right]^2 = \frac{\beta}{2}\left(V_{ov}^2 + v_d V_{ov} + \frac{v_d^2}{4} + 2V_{ov}v_{cm} + v_{cm}^2 + v_d v_{cm}\right) \qquad (2.13a)$$

$$i_2 = \frac{K_N}{2}\left(\frac{W}{L}\right)_1\left[v_I^- - V_{SS} - V_{TN}\right]^2 = \frac{\beta}{2}\left(V_{ov}^2 - v_d V_{ov} + \frac{v_d^2}{4} + 2V_{ov}v_{cm} + v_{cm}^2 - v_d v_{cm}\right) \qquad (2.13b)$$

$$i_o = i_1 - i_2 = \beta\left(v_d V_{ov} + v_d v_{cm}\right) \qquad (2.13c)$$

Assuming that the common-mode interferer and the differential signal have the same frequency, the intermodulation term $v_d.v_{cm}$ is a second-order harmonic component but it is differential and thus is not suppressed when taking the difference of the two currents. For $v_{cm}=V_{pc}\cos\omega t$, the second harmonic distortion can be obtained from equation (2.13) and using the definition in Appendix A:

$$HD_2=V_{pc}/2V_{ov} \qquad (2.14)$$

Note that this cross product effect will be dominated by the quality of the input signal at the first stage in a complete system, for example a filter, provided that the OTA has a good output common-mode rejection. Consequently the common-mode signal that can be allowed at the input of the filter must be low. For example for HD_2 of –50dB and V_{ov}=0.6V, the corresponding maximum tolerated peak common-mode signal at the input is 3.8mV.

2.3.3 Short channel effects

Odd-order harmonics appear due to short channel effects [48]. For short channel devices, the effective carrier mobility is no longer constant, and it is a function of both the longitudinal and transversal electric fields. Considering the degradation of mobility due to these effects and the channel length modulation, the drain current *i* of a transistor in saturation region can be approximated as:

$$i = \frac{\beta}{2}\frac{(v_{GS} - V_{TN})^2}{1+\theta(v_{GS} - V_{TN})}[1+\lambda v_{DS}] \tag{2.15}$$

where $\beta = \mu_0 C_{ox}(W/L)$, $\theta = (1/LE_C)+\theta_0$, and $E_C = v_{sat}/\mu_0$. L is the device channel length, C_{ox} is the oxide capacitance per unit channel area, λ is the output impedance constant, μ_0 is the low-field mobility, v_{sat} is the saturation carrier drift velocity, and E_C is the saturation (critical) longitudinal channel electric field. Note that the value of θ include a fitting parameter θ_0 to model the effect of the transversal electric field [49].

Effective values of θ and λ of $0.4V^{-1}$ and $0.1V^{-1}$, respectively, have been determined for the used technology (0.5μm CMOS) by a best fit to the simulated device characteristics with minimum length. If a differential signal ($v_d/2$) is applied to the inputs, then:

$$v_{GS} - V_{TN} = V_{ov} + (v_d/2) \tag{2.16a}$$

$$v_{DS} = (V_{DD} - V_{SG2}) - V_{SS} + k(v_d/2) = V_{DC} + k(v_d/2) \tag{2.16b}$$

where $V_{DC} = V_{DD} - V_{SS} - V_{SG2}$, and k($\cong -g_{m1}/g_{m2}$) is the gain from the input to node V_z. Substituting (2.16) in (2.15), yields:

$$i_1 = \frac{\beta}{2}\frac{(V_{ov} + v_d/2)^2}{1+\theta(V_{ov} + v_d/2)}\left[1+\lambda V_{DC} + k\lambda\frac{v_d}{2}\right] = \frac{\beta}{2}\frac{1+\lambda V_{DC}}{1+\theta V_{ov}}\frac{(V_{ov}^2 + v_d/2)^2}{1+\eta(v_d/2)}\left[1-\chi\frac{v_d}{2}\right] \tag{2.17}$$

where $\eta = \theta/(1+\theta V_{ov})$, and $\chi = -k\lambda/(1+\lambda V_{DC})$.

Using Taylor series expansion of (2.17), with a differential input $v_d = V_{Peak}\cos\omega t$, the third harmonic distortion becomes:

$$HD_3 = \left| \frac{(\eta + \chi)\left(2\eta - \eta^2 V_{ov} - \frac{1}{V_{ov}}\right)}{32\left(1 - \frac{\eta + \chi}{2} V_{ov}\right)} \right| V_{Peak}^2 \tag{2.18}$$

Neglecting the channel length modulation effect (for k≅-1, λ<θ, and $V_{DC}>V_{ov}$), and substituting by the value of η in (2.18), yields:

$$HD_3 \cong \frac{\theta . V_{Peak}^2}{16 V_{ov}(1+\theta V_{ov})^2 (2+\theta V_{ov})} = \frac{\theta . V_{in\_rms}^2}{8 V_{ov}(1+\theta V_{ov})^2 (2+\theta V_{ov})} \tag{2.19}$$

Fig. 2.11 shows the simulated HD_3 performance of the short-circuit output current of the OTA shown in Fig. 2.8(b) using BSIM models versus the theoretical performance predicted by (2.19).

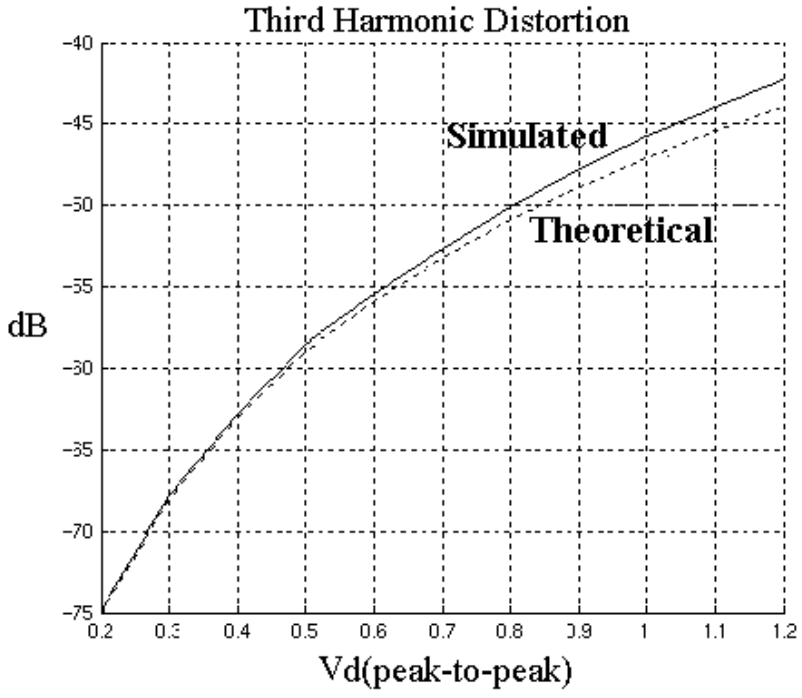


Fig. 2.11 Simulated and theoretical HD_3 performance for V_{ov}=0.6V, θ=0.4V^{-1}

Note that, the smaller θ is the wider the linear range for a given HD_3. This can be accomplished by increasing the length of the channel which at the same time increases the parasitic capacitances. Increasing V_{ov} also improves the linearity at the expense of power consumption.

2.3.4 Nonlinear interaction of differential OTA output signals and CMFB

Another source of nonlinearity is the interaction of the common-mode detector nonlinearity and the output differential signal. This interaction generates nonlinear mixing components at the OTA output [42]. To address this issue, the current i_{CMFB} in Fig. 2.7 can be written, in general, as:

$$i_{CMFB} = \alpha_1 V_{CM} - I_{REF} + i_c + -\alpha_2 v_{od} - \alpha_3 v_{od}^2 = I_{CM} - I_{REF} + i_c + -\alpha_2 v_{od} - \alpha_3 v_{od}^2 \qquad (2.20)$$

where $v_{od} = (v_{OUT}^{+} - v_{OUT}^{-})$, $I_{CM}+i_c = g_{CMFB}(v_{OUT}^{+} + v_{OUT}^{-})/2$, I_{CM} is the dc component that would be the only output of an ideal common-mode detector and it should be compensated by the dc reference current $I_{REF}(=g_{CMFB}V_{REF})$. In this analysis i_c is set to zero since its effect has been already discussed in section 2.3.2. The third and fourth terms of (2.20) are due to mismatches and nonlinearities, respectively, of the common-mode detector. Other higher order terms are neglected since their effect is considered as a third-order effect.

Since the current component $(\alpha_2 v_{od}+\alpha_3 v_{od}^2)$ is fedback to both OTA outputs as common-mode component, it will be attenuated by the action of the CMFB loop, and thus the single-ended output voltages in Fig. 2.7 can be written as:

$$v_{OUT}^{+} = \frac{v_{od}}{2} - \frac{\alpha_2}{1+A} Z v_{od} - \frac{\alpha_3}{1+A} Z v_{od}^2 = \frac{v_{od}}{2} - \delta v_{od} - \alpha v_{od}^2 \qquad (2.21a)$$

$$v_{OUT}^{-} = -\frac{v_{od}}{2} - \delta v_{od} - \alpha v_{od}^2 \qquad (2.21b)$$

where A(=g_{CMFB}.Z.A_{CMD}) is the loop gain of the CMFB, A_{CMD} is the gain of the common-mode detector, Z is the load impedance, and $v_{od} \cong g_m.Z.v_d$.

Note that the single-ended voltages have a common-mode component at the fundamental frequency and a second harmonic component due to the action of the CMFB circuit nonlinearities. The output current i of the next OTA shown in Fig. 2.7, including the short channel effects, the nonlinear mixing components of the fundamental and second-order harmonics, is be obtained by substituting (2.21a) in (2.15) with λ=0 as:

$$i = \frac{\beta}{2}\frac{\left(V_{ov} + v_{od}(0.5-\delta) - \alpha v_{od}^2\right)^2}{1+\theta\left(V_{ov} + v_{od}(0.5-\delta) - \alpha v_{od}^2\right)} = \frac{\beta}{2(1+\theta V_{ov})}\frac{\left(V_{ov} + v_{od}(0.5-\delta) - \alpha v_{od}^2\right)^2}{1+\eta[0.5v_{od}(1-2\delta) - \alpha v_{od}^2]} \qquad (2.22a)$$

Expanding the denominator of (2.22a), while stopping at the third order harmonic, using the formula $(1+x)^{-1} \cong 1-x+x^2-x^3$

$$i \cong \frac{\beta}{2(1+\theta V_{ov})}\left[a_0 + a_1 v_{od} + a_2 v_{od}^2 + a_3 v_{od}^3\right] \times \left[1 + b_1 v_{od} + b_2 v_{od}^2 + b_3 v_{od}^3\right] \qquad (2.22b)$$

where $a_0 = V_{ov}^2$, $a_1 = V_{ov}(1-2\delta)$, $a_2 = \left((0.5-\delta)^2 - 2\alpha V_{ov}\right)$, $a_3 = -\alpha(1-2\delta)$,

$b_1 = -\eta(0.5-\delta)$, $b_2 = \alpha\eta + \frac{\eta^2}{4}(1-2\delta)^2$, $b_3 = -\alpha\eta^2(1-2\delta) - \frac{\eta^3}{8}(1-2\delta)^3$

Assuming that $v_{od} = V_{Peak}\cos\omega t$, we get a general expression for HD_3:

$$HD_{3CMFB} \cong \frac{V_{peak}^2}{4} \times \frac{a_0 b_3 + a_1 b_2 + a_2 b_1 + a_3}{a_0 b_1 + a_1} \qquad (2.23)$$

The previous expression is a general expression for HD_3 including the nonlinearity due to the short channel effects and the common-mode feedback detector. A case study of using this expression is discussed next.

Considering the nonlineraities of the common-mode detection as given by (2.5) and assuming perfect matching (δ=0), an expression of HD_3 for the OTA shown in Fig. 2.9, as a special case of the OTA shown in Fig. 2.7, can be obtained by substituting the corresponding values in (2.23). First, we calculate the term α due to the nonlinear common-mode detection. According to (2.5), we have:

$$i_{CMFB} = 0.5(i_1 + i_2) - I_{REF} = 0.5\beta.V_{ov}^2 - I_{REF} - \alpha_3.v_d^2 = I_{CM} - I_{REF} - \alpha_3.v_d^2$$

where $\alpha_3 = -K_P W_1 / 8L_1 = -g_m / 8V_{ov}$.

Considering the short channel effects and using Taylor series expansion of (2.15) with λ=0, we get a more accurate value of α_3 given by:

$$\alpha_3 = -\frac{K_P}{8}\left(\frac{W}{L}\right)_1 \frac{1}{(1+\theta V_{ov})^3} = \frac{-g_m}{8V_{ov}(1+\theta V_{ov})(1+0.5\theta V_{ov})} \tag{2.24}$$

According to (2.21a), for $g_{CMFB}=g_m$ and $A_{CMD}=\frac{(W/L)_{\overline{M}_3}}{(W/L)_{M_3}} = \frac{(W/L)_{\overline{M}_4}}{(W/L)_{M_4}}=1$, we have:

$$\alpha = \frac{\alpha_3}{1+A} Z = \left(\frac{A}{1+A}\right)\left(\frac{-1}{8V_{ov}(1+\theta V_{ov})(1+0.5\theta V_{ov})}\right) \tag{2.25}$$

Substituting the values of η and α in (2.23), and after some algebraic manipulations, we can write:

$$HD_{3CMFB} \cong \frac{\theta.V_{Peak}^2}{16V_{ov}(1+\theta V_{ov})^2(2+\theta V_{ov})}\left[1+\left|\frac{A}{1+A}\right|\frac{1}{\theta V_{ov}(1+0.5\theta V_{ov})}\right] = HD_3 \times F \tag{2.26}$$

where HD_3 is described by (2.19) and the ideal linear value of F is one (0dB). F describes the linearity deterioration factor due to interaction of the common-mode detector nonlinearity and the input differential signal. Fig. 2.12 shows the value of F in dB as a function of |A| for two different values of θV_{ov}.

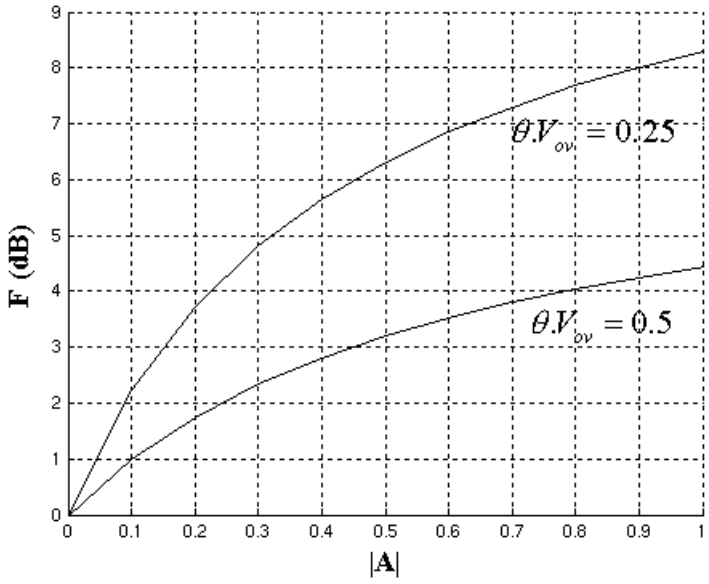


Fig. 2.12 Effect of |A| on linearity deterioration factor F due to the nonideal CMFB

Consider only the integrated thermal noise power, and using equations (2.10b) and (2.26), the following expression for the signal-to-noise ratio (SNR) can be obtained (for F=1 and B=1):

$$SNR = 10\log\left[\frac{V_{in\_rms}^2}{V_{n\_rms}^2}\right] \cong 10\log\left[\frac{3.HD_3.V_{ov}(1+\theta V_{ov})^2(2+\theta V_{ov}).g_{m1}}{2.BW.KT.\theta\left(1+\frac{g_{m2}+2g_{m3}+2g_{m4}}{g_{m1}}\right)}\right] \quad (2.27)$$

For a given HD_3, the maximum input voltage, and consequently the SNR, can be increased by increasing V_{ov}. The transconductance g_{m1} needs also to be maximized to reduce the noise contribution of subsequent transistors. There are a number of possible OTA design procedures based on the specifications. A particular design procedure for the OTA is shown in Fig. 2.13 for given specifications of g_m, excess phase, noise, and HD_3.

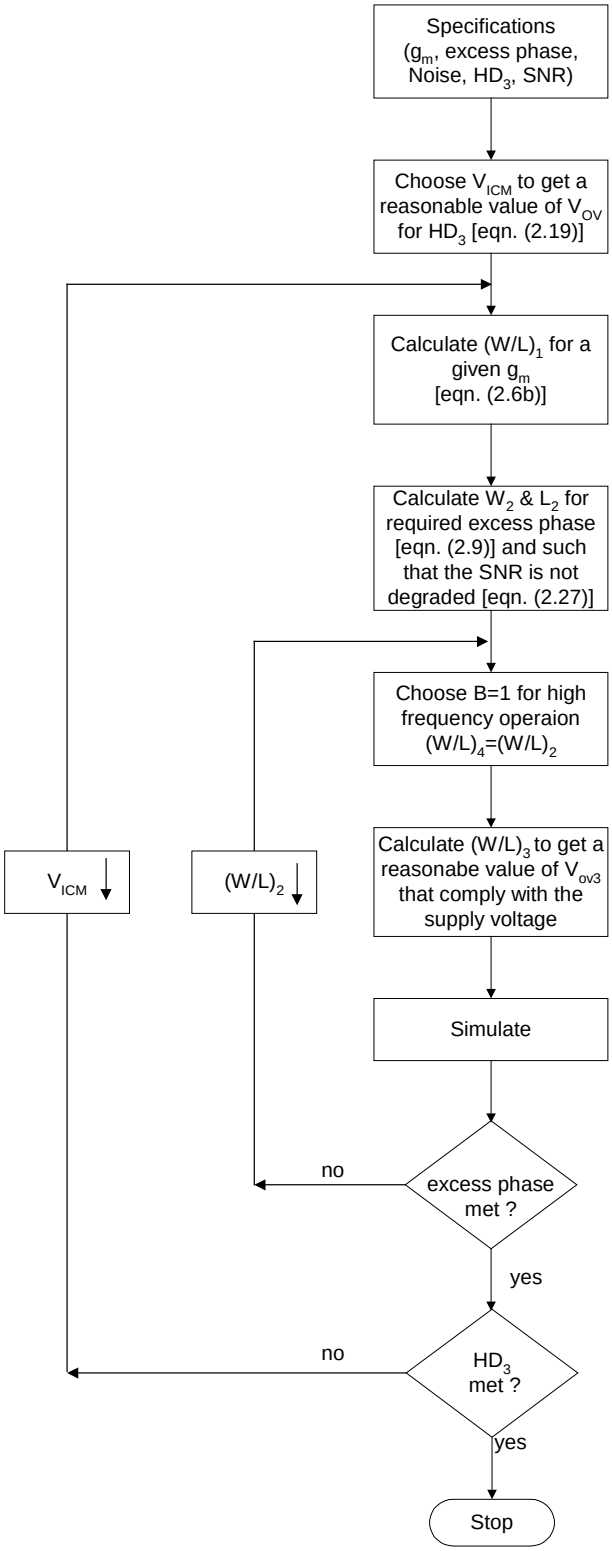


Fig. 2.13 Flow chart of an OTA design procedure

Illustrative examples. The design examples assumes AMI 0.5μm CMOS process with $|V_{TP}|$=1V, K_P=36μA/V^2, K_N=116μA/V^2, and C_{ox}=2.5fF/μm^2.

Case 1. In the first example, the design goals are a transconductance value of 1mS, $\Delta\phi$ less than 0.1^0@100MHz, and HD_3<-40dB for a $1V_{pp}$ input differential signal. For the proposed OTA of Fig. 2.8(b), B is chosen to be 1, i.e., $(W/L)_4=(W/L)_2$, and minimum length is used for transistors for high frequency operation. This results in θ of $0.4V^{-1}$, according to simulations. To obtain an HD_3<-40dB for a $1V_{pp}$ input differential signal, the value of V_{ov} can be calculated according to equation (2.19) to be greater than 0.6V. For a supply voltage of 1.65V, this results in a common-mode voltage V_{REF} of 0V. The value of $(W/L)_1$ for g_m=1mS (as required by the filter of section 2.5) according to equation (2.6b) is calculated to be 46. For L_1= 0.5μm, this leads to W_1 of 23μm and I_{DC} of 300μA. According to (2.9) the excess phase is less than 0.1^0@100MHz for W_2<300μm. Since g_{m2} should be reduced according to (2.27) in order not to degrade the SNR, W_2 is chosen as the minimum value in order to comply with the supply voltage, i.e., a reasonable value for V_{ov2}. For V_{ov2}=0.5V, $(W/L)_2$ can be calculated to be 20, i.e, W_2=10μm. For V_{ov3}=0.5V, $(W/L)_3$ can be also calculated to be 60, i.e, W_3=30μm. According to (2.27), this results in an SNR of 65dB for the OTA.

Case 2. In the second example, the design goals are more relaxed on the transconductance value and more stringent requirements on linearity. For this design the specifications are a transconductance value of 100μS and HD_3<-60dB for a $1V_{pp}$ input differential signal. In this design B is also chosen to be 1, but minimum length cannot be used for input transistors to be able to achieve the linearity requirements. To obtain an

HD_3<-60dB for a $1V_{pp}$ input differential signal for V_{ov}=0.5V, the value of θ can be calculated according to equation (2.19) to be less than $0.07V^{-1}$. Since θ is inversely proportional with L, the length of the input transistors is chosen to be 6 times the minimum dimension which results in $\theta = 0.06V^{-1}$. The value of $(W/L)_1$ for g_m=100μS according to equation (2.6b) is calculated to be 6. For L_1=3μm, this leads to W_1 of 18μm and I_{DC} of 25μA. W_2 is chosen as the minimum value in order to comply with the supply voltage, i.e., a reasonable value for V_{ov2}. For V_{ov2}=0.3V, $(W/L)_2$ is be calculated to be 6, i.e., W_2=6μm with L_2=1μm. For V_{ov3}=0.3V, $(W/L)_3$ is 16, i.e., W_3=16μm and L_3=μm.

Tuning. The proposed OTA can be tuned by changing the common-mode voltage V_{ICM}. The main disadvantage, as in the case of conventional OTA based on a differential pair with a tail current source, is the variation of the linearity performance with changing the bias conditions. However, this effect is less severe for pseudo differential structures, where SNR is proportional to V_{ov}, than for fully differential structures with tail current source, where SNR is proportional to V_{ov}^2 [50]. The tunability of ±35% of the OTA, by varying the CM voltage, is shown in Fig. 2.14(a), while Fig. 2.14(b) shows the corresponding 10dB variation HD_3 performance HD_3 performance for a $500mV_{pp}$ differential input signal. These results are in good agreement with equation (2.19). Fig. 2.14(c) shows the effect of tuning on the excess phase Δϕ at 100MHz.

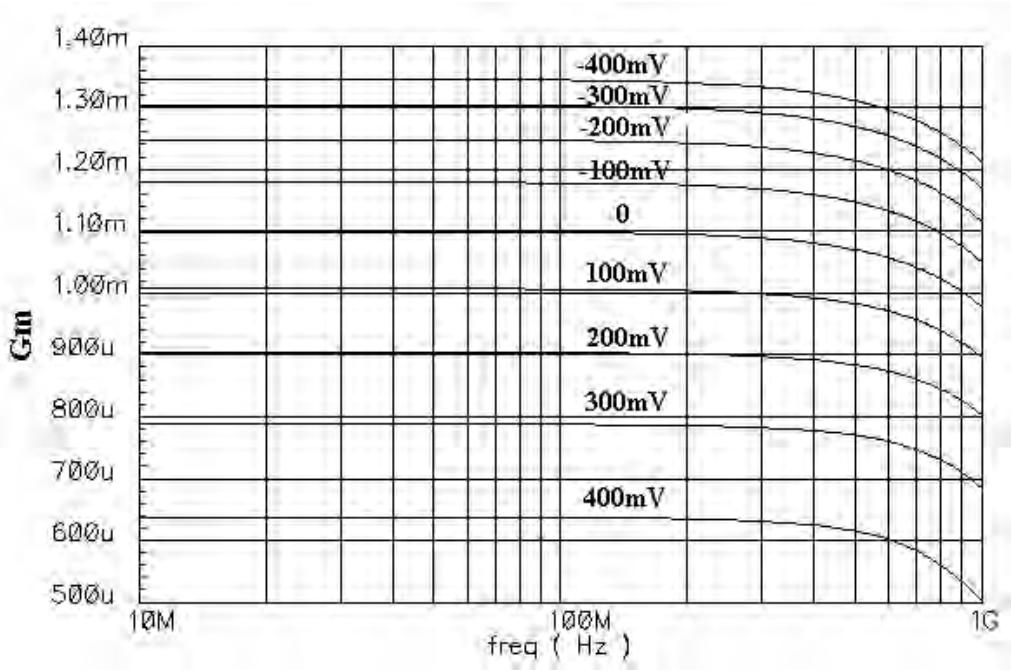


Fig. 2.14(a) OTA tuning by changing CM voltage V_{ICM}

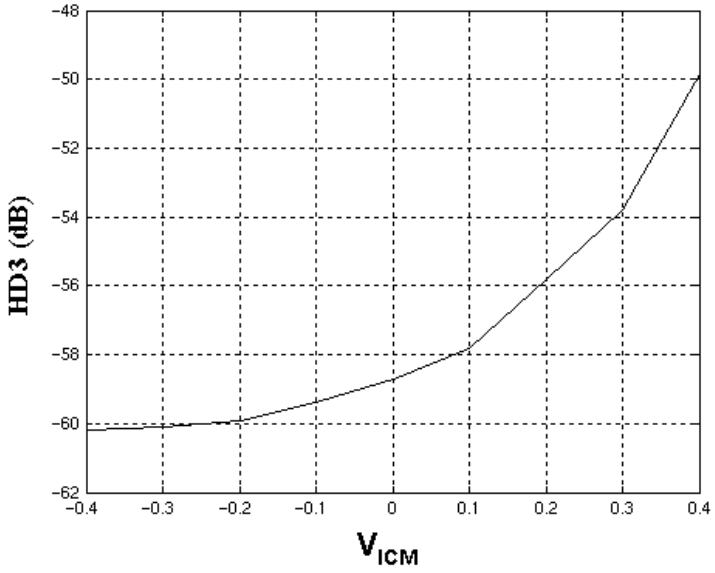


Fig. 2.14(b) Effect of tuning on HD_3 performance

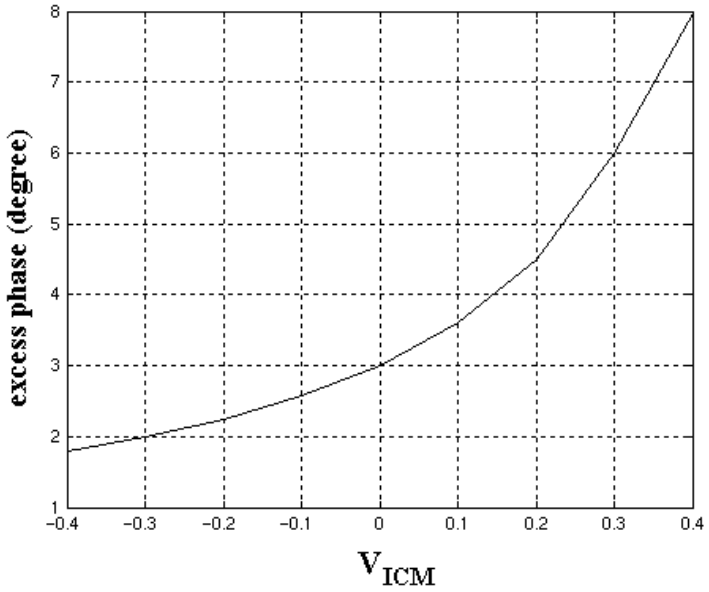


Fig. 2.14(c) Effect of tuning on excess phase

In practice, the CM voltage of the OTAs is forced by the action of the CMFB circuit to be equal to the reference voltage V_{REF} [see Fig. 2.9]. Note that this reference voltage is generated using the reference current I_{REF} and the diode connected transistor M_1 and $V_{REF}=V_{DD}-|V_{TP}|-V_{ov}$. Accordingly, the common-mode dc level tracks any supply voltage variation and this will not translate into transconductance variation.

2.4. CMFB Loop Design Considerations

In this section various design considerations for the CMFB loop are discussed.

2.4.1 Common-Mode Loop and Stability Conditions

The open loop gain of the CMFB A_{CMFB} in Fig. 2.9, can be calculated as (for B=1):

$$A_{CMFB}(s) = \frac{V_{cm}}{V_{in}}(s) = A_{CMD} \cdot \frac{g_{m1}}{g_{m2} + sC_Z} \cdot \frac{g_{m2}}{g_{m3} + sC_X} \cdot \frac{g_{m3}}{g_o + sC_L} = \frac{g_{CMFB}(s)}{g_o + sC_L} \qquad (2.28)$$

A_{CMFB}, determined as shown in Fig. 2.15, should be made as high as possible at dc, and its bandwidth should be as high as the differential-mode bandwidth. The CMFB loop is compensated for stability purposes by the load capacitance C_L, which is also used for differential-mode operation.

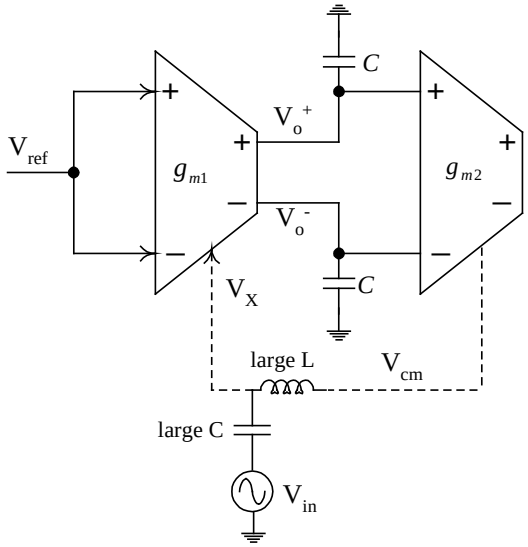


Fig. 2.15 Setup to determine the open loop gain of the CMFB

To ensure sufficient phase margin in the CMFB loop it is required that the following constraints are satisfied.

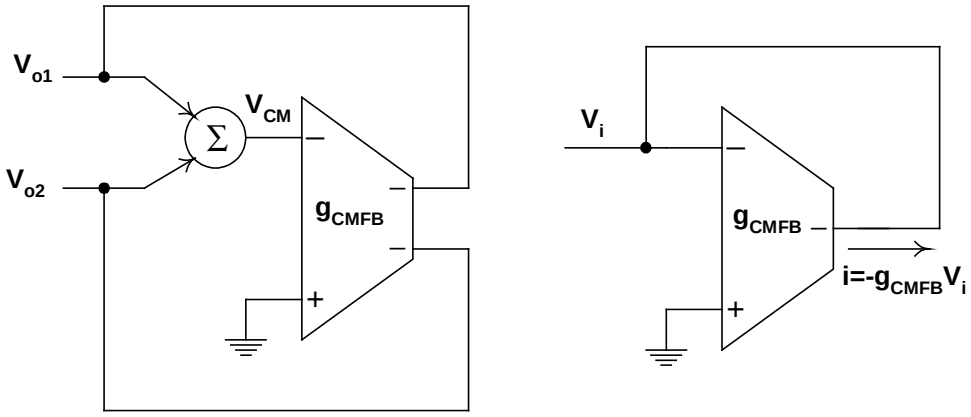
$$\omega_{nd1} = \frac{g_{m2}}{C_Z},\ \omega_{nd2} = \frac{g_{m3}}{C_X} > 2A_{CMD} \cdot \frac{g_{m1}}{C_L} \qquad (2.29)$$

where $A_{CMD} = (W/L)_3 / (W/L)_3 = (W/L)_4 / (W/L)_4$. Note that for differential-mode gain we have to consider only one parasitic pole ω_{nd1}, see Fig. 2.9. For the differential

mode gain, it has to be guaranteed that ($g_{m1}/C_L << \omega_{nd1}$) otherwise the integrator excess phase error is huge [see equations (2.8) and (2.9)], therefore the stability of the CMFB loop is also guaranteed.

2.4.2 Common-Mode Gain

A general CMFB loop is shown in Fig. 2.16(a). The average of the two output voltages V_{o1} and V_{o2} is compared with the reference voltage (ground in this case), and a correcting current is added/subtracted at the output branches to close the loop. This is equivalent to a voltage controlled current source in a unity gain configuration, as shown in Fig. 2.16(b), which represents a grounded impedance of value $1/g_{CMFB}$. Thus, the CMFB is idealy transparent to differential signals and acts at low frequencies as a resistor of value $1/g_{CMFB}$, the small signal common-mode feedback transconductance, for common-mode signals.



(a) (b)

Fig. 2.16(a) Loop for CM signals (b) A VCCS in a unity gain configuration

Hence the common-mode gain of the OTA shown in Fig. 2.9, including the CMFB circuit, can be determined from Fig. 2.16(c) to be:

$$A_{CM}(s)=\frac{v_{ocm}}{v_{icm}}(s)=\frac{\dfrac{g_{m1}.g_{m2}}{g_{m2}+sC_Z}-\dfrac{g_{m1}}{g_{m2}+sC_Z}\dfrac{g_{m2}.g_{m3}}{g_{m3}+g_0+sC_X}}{g_{CMFB}(s)+g_0+sC_L}$$
$$=\frac{g_{m1}.g_{m2}(g_0+sC_X)}{(g_{m2}+sC_Z)(g_{m3}+sC_X)\left[g_{CMFB}(s)+g_0+sC_L\right]} \qquad (2.30)$$

where C_X is the total parasitic capacitance at node V_X, C_L is the load capacitance, and g_0 is the output conductance. Note that A_{CM} at low frequency is much less than unity because g_{CMFB} is large; this is a result of the action of both CMFB and CMFF circuits. At high frequency, the low frequency zero degrades the rejection to common-mode signals.

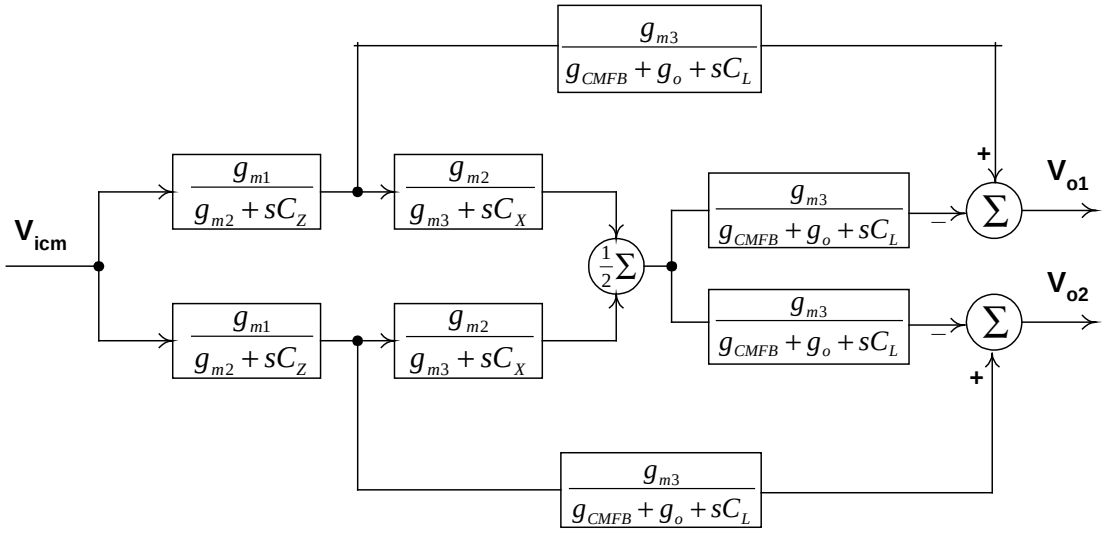


Fig. 2.16(c) Conceptual diagram to calculate common-mode gain

According to (2.7b) and (2.30), the CMRR can be written as:

$$CMRR(s)=\frac{A_{DM}(s)}{A_{CM}(s)}=\frac{(g_{m3}+sC_X)\left[g_{CMFB}(s)+g_0+sC_L\right]}{(g_0+sC_X)(g_0+sC_L)} \qquad (2.31a)$$

$$CMRR(0) = \frac{g_{m3} \cdot g_{m1}}{g_0^2} \tag{2.31b}$$

Fig. 2.17(a) shows the setup used to measure the step response of the CMFB loop. It consists of two OTAs in cascade forming an integrator and a common-mode feedback detector. A common-mode step current I_{cm} of 15% of the bias current is applied at each output branch of the integrator. The output common-mode volatge, $V_{OCM}=0.5(V_o^+ + V_o^-)$, is shown in Fig. 2.17(b). Note that For the case of the CMFF alone the output voltage is not fixed.

For the other two cases the dc value of the output voltage is fixed to the required reference value (except for an offset of 50mV). Note that the transient response using both CMFB and CMFF techniques is better (lower overshoot and less settling time) than using CMFB alone. Fig. 2.17(c) shows the open loop gain of the CMFB with a 63.6^0 and 11dB of phase margin and gain margin, respectively.

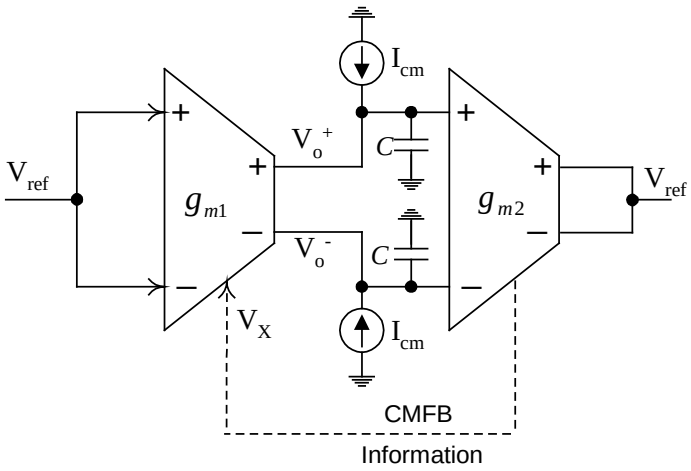


Fig. 2.17(a) Setup to measure the step response of the CMFB due to the current step I_{cm}

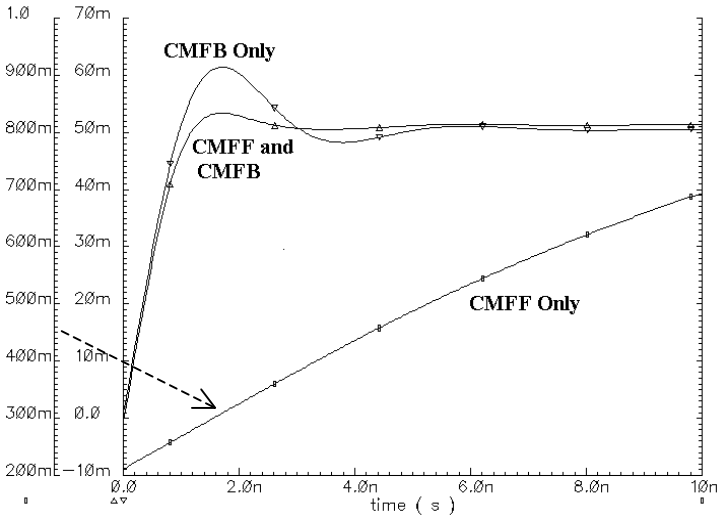


Fig. 2.17(b) Transient response applying a common-mode current step at the output

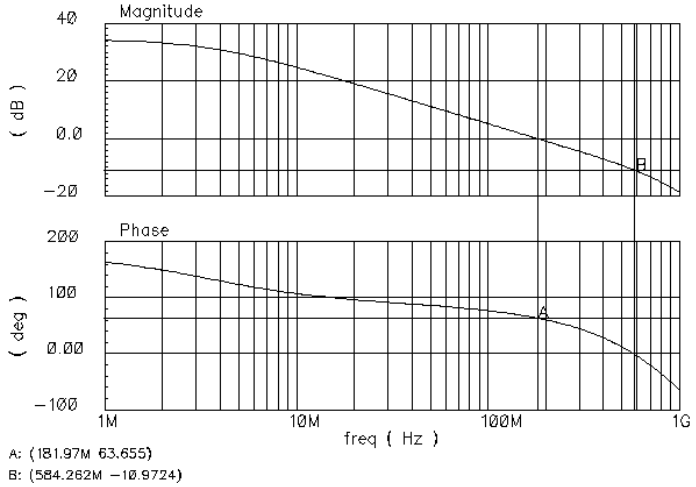


Fig. 2.17(c) Open loop gain of the CMFB

The proposed OTA in Fig. 2.9 is suitable for low voltage applications with a minimum required supply voltage of V_{DD_min} and common-mode range (CMR) given by:

$$V_{DD\_min} = \max \{(V_{TN}+V_{ov1}+2V_{ov2}+V_{Peak}), (|V_{TP}|+2V_{ov3}+2V_{ov4})\} \quad (2.32)$$

$$V_{SS}+V_{ov2}+V_{TN}-|V_{TP}|<CMR<V_{DD}-|V_{TP}| \quad (2.33)$$

2.5. Linear Phase Filter

A fourth order linear phase Bessel-Thomson OTA-C filter using the proposed OTA has been fabricated and tested. The requirement is a group delay ripple less than 3% for frequencies up to $1.5\times f_0$, where $f_0 = 50MHz$. A fourth order filter is needed to satisfy the required specifications. The required normalized transfer function is given by:

$$H(s) = \frac{9.14013}{s^2+5.79425s+9.14013}.\frac{11.4878}{s^2+4.207585s+11.4878} \quad (2.34)$$

$\omega_{01} = 3.389,\ Q_1 = 0.806,\ \omega_{02} = 3.023,\ Q_2 = 0.522$

The -3dB cut-off frequency of the low pass response filter is $f_{-3dB}=2.13\times f_0=106MHz$. The block diagram of the filter with the required CMFB arrangement is shown in Fig. 2.18. The filter is composed of two biquadratic sections. The values of the transconductances and capacitors used are given in Table 2.3.

Table 2.3 Transconductances and capacitors values

Parameter	**Value**	**Parameter**	**Value**
g_{m1A}	1065 μS	g_{m2A}	1320 μS
g_{m1B}	1065 μS	g_{m2B}	2040 μS
C_{L1}	1.0 pF	C_{L2}	1.12 pF

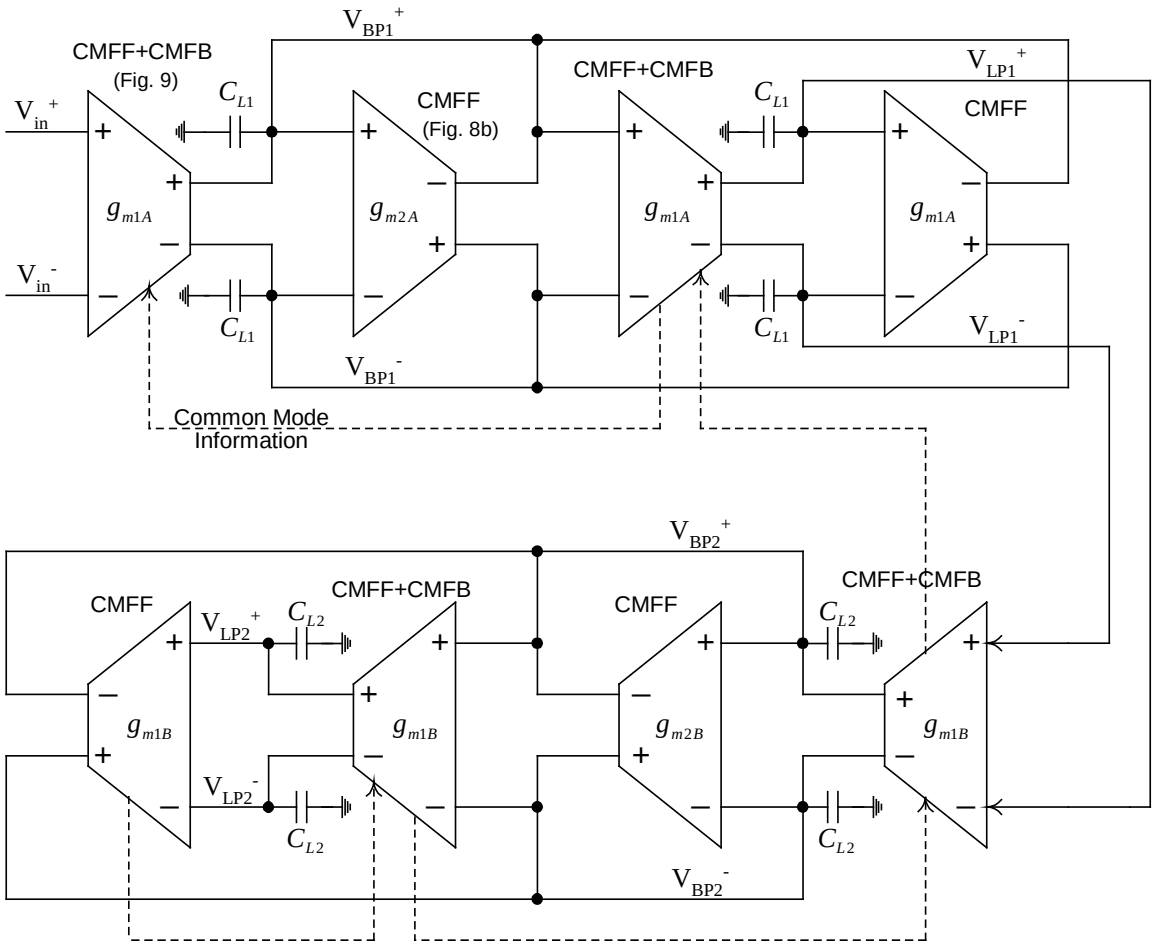


Fig. 2.18 A 4th order linear phase filter architecture

The output common-mode level needs to be fixed only once for any number of OTAs sharing the same output. Thus, some of the fully fledged OTAs (with CMFB and CMFF) may be replaced by ones with CMFF only as that shown in Fig. 2.8(b). For instance, g_{m2A}, g_{m2B}, the last stage of the first biquad, and the last stage of the second biquad do not need to have a CMFB since their outputs are shared with other OTAs which will fix the output dc level of the output. Transconductances g_{m2A} and g_{m2B} may

not need a CMFF either, and they could be replaced by conventional ones as that shown in Fig. 2.6(a) since the output of the previous transconductances can be sensed somewhere else (by another OTA). Note that both the CMRR and PSRR could be deteriorated if the CMFF is not employed.

All the OTA non-idealities affect the accuracy of the filter and consequently the group delay ripple. Those include finite OTA output impedance, finite input impedance, excess phase due to the internal parasitic poles, and nonlinear voltage to current conversion. The error in the group delay, $\Delta\tau(\omega)$, can be written as [25]:

$$\frac{\Delta\tau}{\tau}(\omega)=\left[S_{Q_1}^{\tau_1}(\omega).\frac{\Delta Q_1}{Q_1}+S_{\omega_{01}}^{\tau_1}(\omega).\frac{\Delta\omega_{01}}{\omega_{01}}\right]\frac{\tau_1}{\tau}+\left[S_{Q_2}^{\tau_2}(\omega).\frac{\Delta Q_2}{Q_2}+S_{\omega_{02}}^{\tau_2}(\omega).\frac{\Delta\omega_{02}}{\omega_{02}}\right]\frac{\tau_2}{\tau} \qquad (2.35)$$

where $S_X^Y=\frac{(\partial Y/\partial X)}{(Y/X)}$. Thus the overall error in the group delay depends on the corresponding sensitivities and the variations of Q and ω_0, of the two biquads, due to the previously mentioned non-idealities. Fig. 19(a) and 19(b) show the sensitivity functions for the two biquadratic sections. Notice that if $\Delta\omega_{01}$ and $\Delta\omega_{02}$ are correlated, their corresponding errors are partially compensated, leading to a fairly constant group delay deviation, up to $f \cong 2f_0$, which can be overcome by the use of an automatic tuning system. This is not the case of ΔQ deviations, thus more design effort is required to minimize these errors. To push the value of the non-dominant poles to high frequency N-type current mirrors are used as shown in Fig. 2.9.

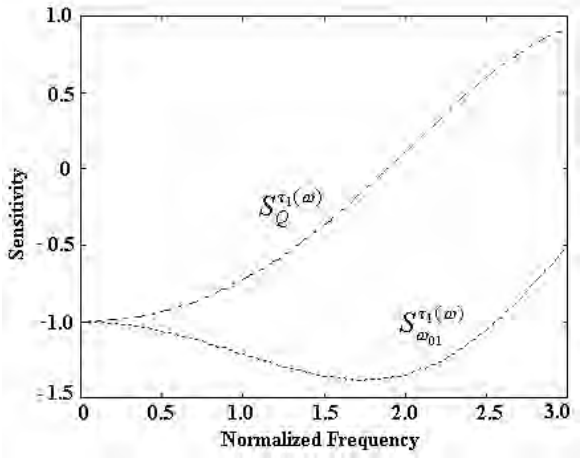


Fig. 2.19(a) Sensitivity functions for Biquad 1

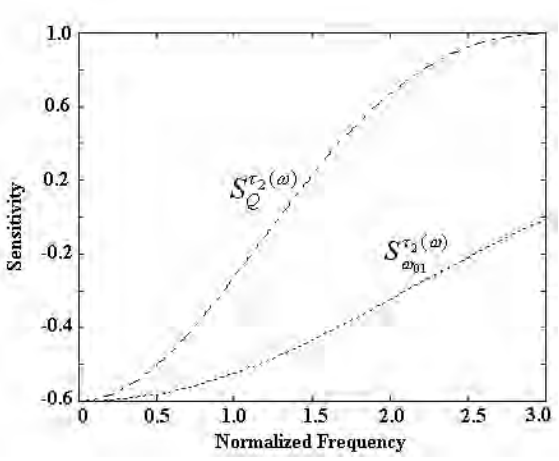


Fig. 2.19(b) Sensitivity functions for Biquad 2

2.6. Measurement Results

An integrator built using the proposed OTA, and the 4th order linear phase filter have been fabricated in the AMI 0.5μm CMOS process available through MOSIS. The chip micrograph is shown in Fig. 2.20. The integrator (g_m=1065μS, C_L=2pF) occupies an area of 0.035 mm^2. The filter occupies an area of 450x350 μm^2. The power supply used is ±1.65V.

Fig. 2.21(a) and 2.21(b) show the measured differential- mode gain and common-mode gain, respectively, for the integrator. The measured CMRR defined as the ratio of the differential mode gain to the common-mode gain [48], is 58dB at low frequencies. The measured input referred noise spectral density is $9.8\,nV/\sqrt{Hz}$ at 50MHz.

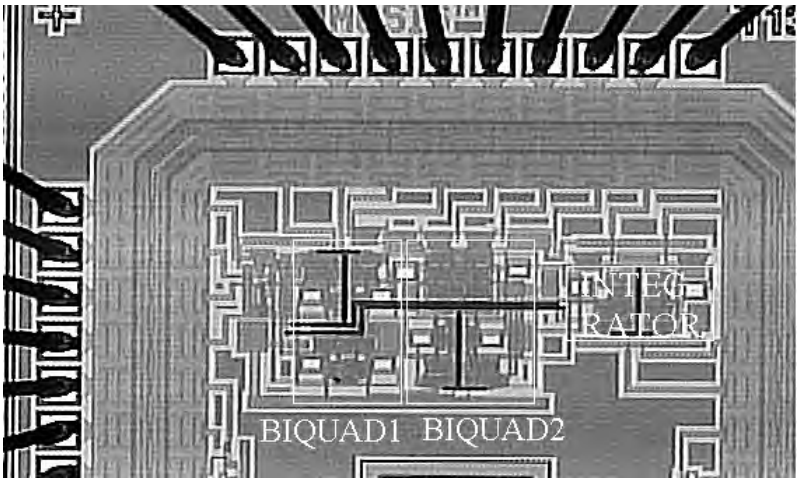


Fig. 2.20 Chip micrograph

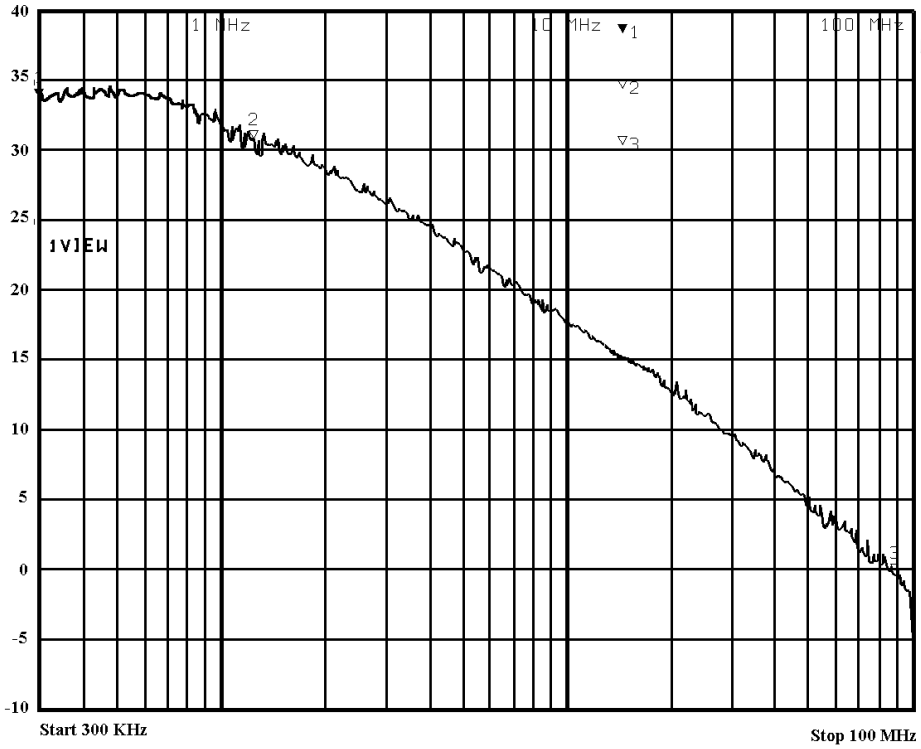


Fig. 2.21(a) Integrator differential-mode gain

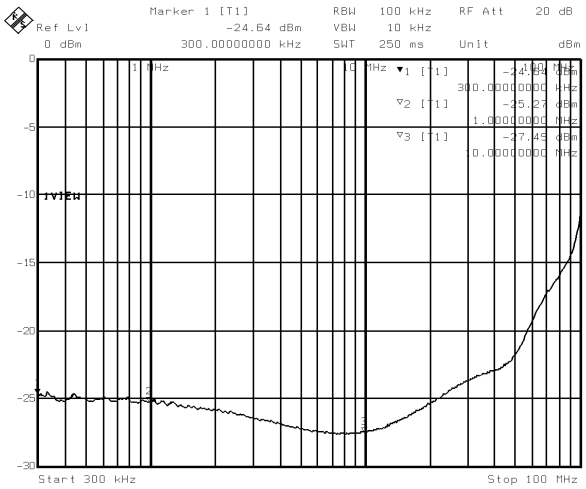


Fig. 2.21(b) Integrator common-mode gain

Fig. 2.22 shows the OTA output spectrum, at one of the output terminals, for a differential input signal of amplitude 900mV_{pp} and frequency 30MHz. HD_2 is small (-37dB) due to the even-order harmonic cancellation of the CMFF, and HD_3 is measured around –43dB.

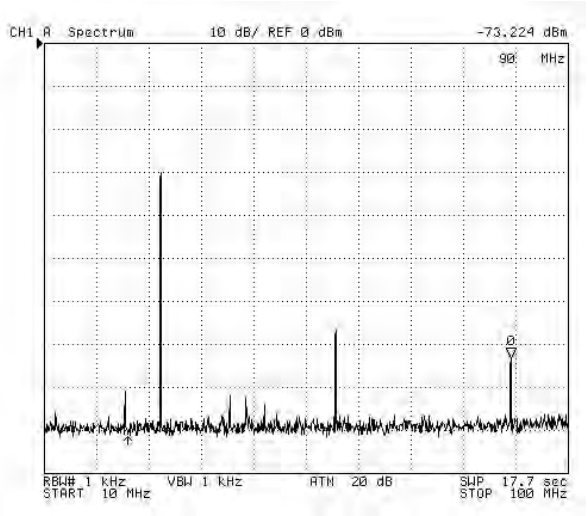


Fig. 2.22 OTA output spectrum, at one of the output terminals, for a 0.9V_{pp} 30 MHz input

The measurement setup for the transfer function and the intermodulation distortion of the filter are shown in Fig. 2.23 and Fig. 2.24, respectively.

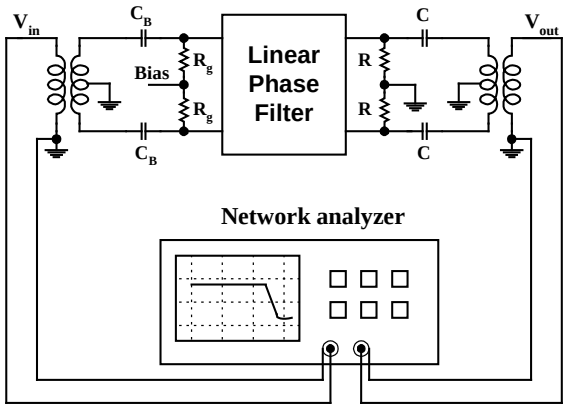


Fig 2.23 Measurement setup for transfer function

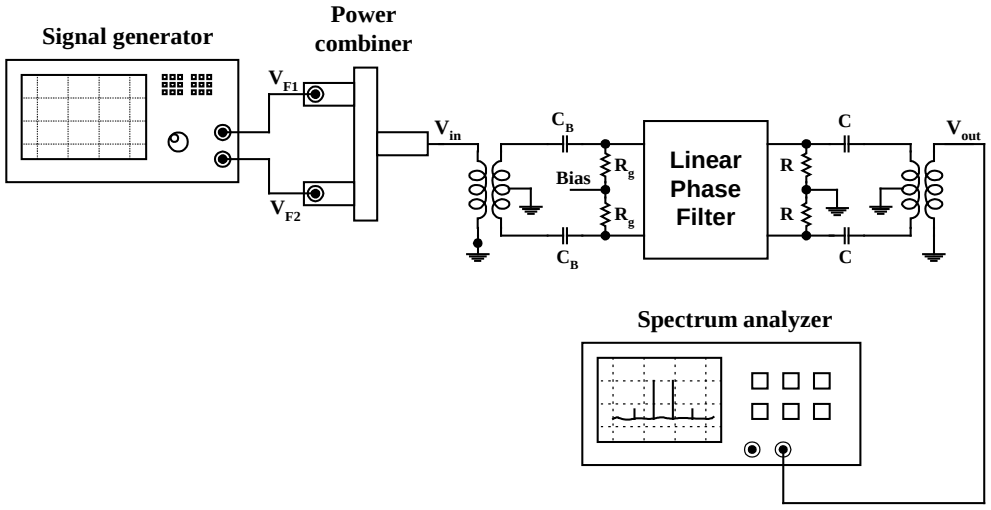


Fig 2.24 Measurement setup for intermodulation distortion

Fig. 2.25(a) and 2.25(b) show the measured magnitude and phase responses of the filter, respectively. The -3dB cut-off frequency is 100MHz. The group delay is shown in

Fig. 2.26; measured group delay ripple is about 3% for frequencies up to 100MHz and less than 10% for frequencies up to 120MHz.

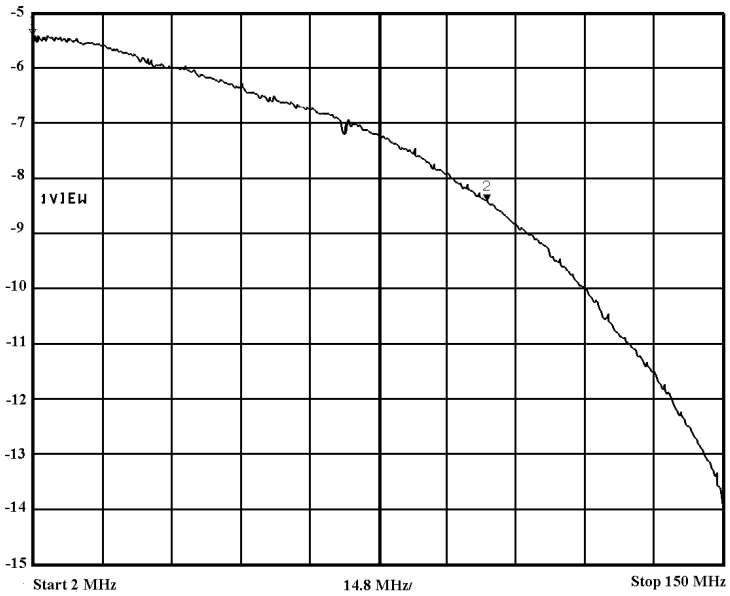


Fig. 2.25(a) Magnitude of filter frequency response

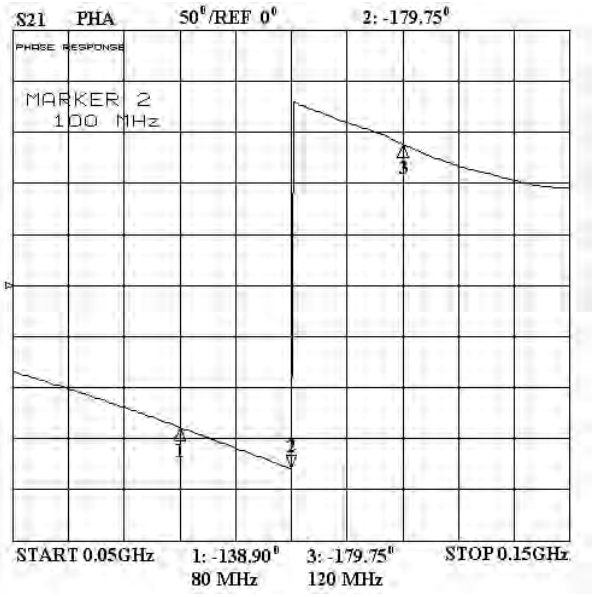


Fig. 2.25(b) Phase of filter frequency response

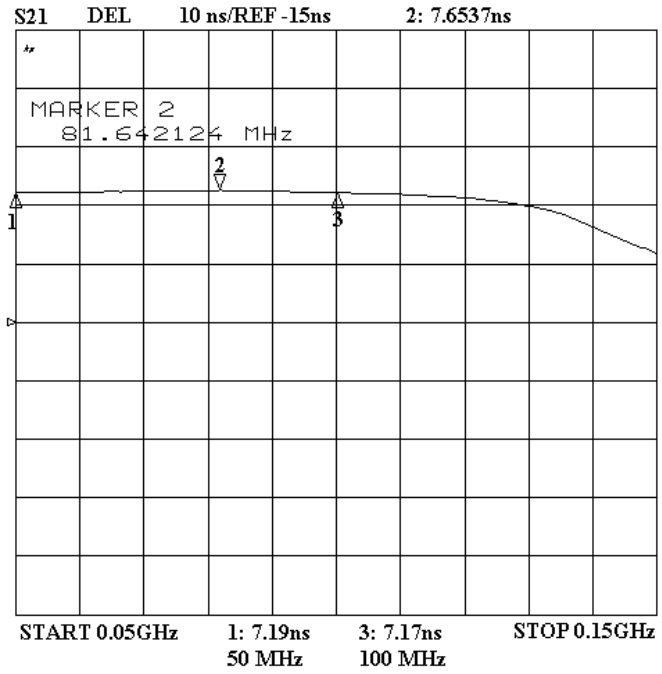


Fig. 2.26 Filter group delay

Fig. 2.27 shows the filter output spectrum for a differential input signal of amplitude 350mV$_{pp}$ and frequency 30MHz (approximately $f_{3dB}/3$); HD_3 is measured around –49dB for these settings. The result of an intermodulation distortion test is shown in Fig. 2.28 for two-tones applied at 99MHz and 101MHz with an amplitude of 350mV$_{pp}$ each. The IM_3 is about 40dB and is fairly constant over the whole passband. The total output noise generated in the bandwith from 0 to 100MHz is about 700μV$_{rms}$. This corresponds to 45dB of dynamic range for 0.5% THD at 30MHz.

The measured CMRR, PSRR$^+$, and PSRR$^-$ at 10MHz is 45dB, 26dB, and 35dB, respectively, 32dB, 21dB, and 28dB, respectively, at 50MHz, and 26dB, 16dB, and

22dB, respectively, at 100MHz. The filter consumes 26mA. Table 2.4 contains a summary of different filter performance parameters compared with previously reported works in [23-24].

Table 2.4 Filter performance parameters

	[23]	**[24]**	**This Work**
Filter order & type	7^{th} Order 0.05^0 Equirriple	7^{th} Order 0.05^0 Equirriple with filter boost	4^{th} Order Bessel
Cut- Off frequency	50 MHz	100 MHz	100 MHz
Ripple on group delay	< 2% @ $.2f_{3dB} < f < 1.5f_{3dB}$	< 5% @ $f < 2f_{3dB}$	< 3% @ $f < f_{3dB}$
Max input signal for 0.5% THD	200 mV_{p-p}	100 mV_{p-p}	350 mV_{p-p}*
THD	-46 dB	-46 dB	-46 dB
Output noise level	1.7 mV_{rms}	N/A	700 μV_{rms}
Dynamic range @ THD=-46dB	32 dB	> 40 dB	45 dB
Supply voltage	3 V	3 V	3.3 V
Current consumption	27 mA	40 mA	26 mA
Technology	0.72 μm CMOS	0.29 μm BiCMOS	0.5 μm CMOS

* The maximum differential input signal is 500mV_{p-p} for 1% THD

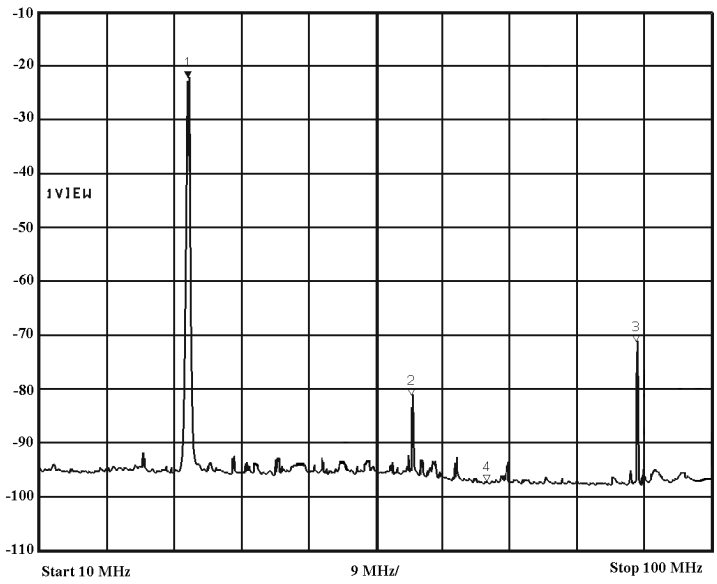


Fig. 2.27 Filter output spectrum for a 350 mV_{pp} 30 MHz input signal (THD=0.5%)

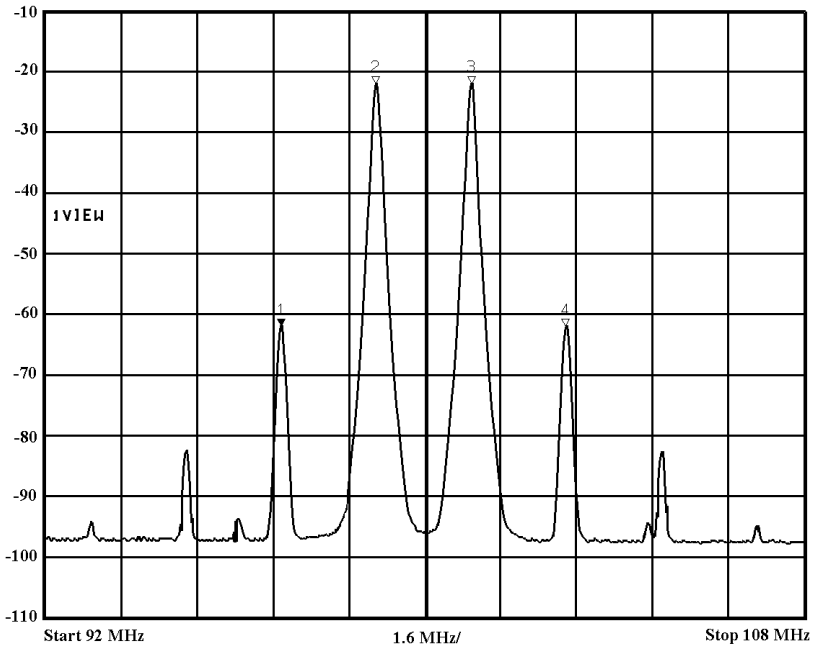


Fig. 2.28 Two-tone intermodulation distortion test (IM_3=40dB)

2.7. Conclusions

A pseudo differential fully symmetric fully balanced OTA architecture has been presented. It has been shown that an OTA with inherent CMFF structure made it easier to incorporate the CMFB arrangement. This is done at minimum cost of area and power consumption. The same principle can be applied to any OTA with CMFF to incorporate the detection of the common-mode information of the previous stage for CMFB stabilization.

The linearity and noise design considerations have been discussed. General nonlinear effects in pseudo-differential OTAs with CMFB have been described. The nonlinearity effects due to the interaction of the nonlinear common-mode signal of the CMFB circuit and the differential-signal have been determined. Other nonlinearity sources such as transistor mismatches, cross product of differential and common-mode signals, short channel effects have been also theoretically derived. To invoke the theory, the proposed pseudo-differential fully symmetric fully balanced OTA architecture has been taken as an example.

A 4^{th} order 100MHz linear phase filter using the proposed transconductance has been designed. The group delay ripple is 3% for frequencies up to the filter cut-off frequency. The measured IM_3 is 40dB over the whole passband for two tones of $350mV_{p-p}$ each. The filter's active area is $0.15mm^2$ in 0.5μm CMOS process and operates from ±1.65V power supply. The measured results assure the good performance of the proposed transconductance building block and its suitability for high frequency operation.

CHAPTER III

A DUAL-MODE LOW-PASS FILTER FOR BLUETOOTH AND IEEE 802.11B

3.1. Motivation and Background

The market of wireless communications had a tremendous growth over the past few years. Wireless technology is now capable of reaching virtually every location on earth. Hundreds of millions of users exchange information every day using cellular phones and other wireless communication products. There has been also a vast growth, over the last decades, of very large scale integration (VLSI) electronic devices like desktop and laptop computers, personal digital assistants (PDA), cellular phones, printers, scanners, digital cameras and even home appliances.

The demand grows more for wireless communication, beyond voice transfer, to personal and business computing enabling these electronic devices to communicate wirelessly via short-range connections. Information data transfer between these devices would enable people to access and share information on a global scale literally anywhere they go.

Bluetooth [51] technology is a universal specification that enables short-range (about 30feet) wireless connections between cordless or mobile phones, modems, headsets, PDAs, computers, printers, projectors, etc., on a globally available band (2.4GHz) for worldwide compatibility. The technology enables the design of low power, small sized

low cost radios that can be embedded in existing (portable) devices. The Bluetooth system is operating in the 2.4GHz Industrial Scientific Medicine (ISM) band between 2400MHz and 2483.5MHz. The modulation scheme employed is Gaussian Frequency Shift Keying (GFSK) with an instantaneous bit rate of 1Mb/s and channel spacing of 1MHz.

Another way that has been widely used nowadays to access and share information is networking. The power of networking and collaborative, distributed computing has been realized during the last decades through standard local area network (LAN) protocols, such as Ethernet, that operate at fairly high speeds with inexpensive connection hardware. This can bring digital networking to almost any computer. IEEE 802.11b is the wireless extension of wired Ethernet. The major motivation and benefit from wireless local area networks (WLAN) is increased mobility and flexibility.

The IEEE 802.11b specification [52] allows for the wireless transmission of approximately 11Mb/s of raw data at indoor distances from several dozen to several hundred feet and outdoor distances of several to tens of miles. It shares the same 2.4GHz band with Bluetooth.

The coexistence of a dual-standard receiver for both Bluetooth and IEEE 802.11b, combining the capabilities of both technologies, paves the way for new devices and applications that are limited only by our imagination. Some leading manufactures such as Intersil Corp. and Silicon Wave Inc. are ready to demonstrate the first radio transceiver circuitry that supports both IEEE 802.11b WLAN and Bluetooth

communications. The chip set enables the seemingly simultaneous, i.e., in the same RF frequency band, operation of both networks without mutual interference.

This chapter presents the design of a dual-mode low-pass channel selection filter to be used in a dual-standard direct conversion receiver for Bluetooth and IEEE 802.11b, as shown in Fig. 3.1. The design is carried out in the IBM 0.25μm BiCMOS technology and the filter operates form 2.5V single supply. A digital automatic tuning system is also implemented.

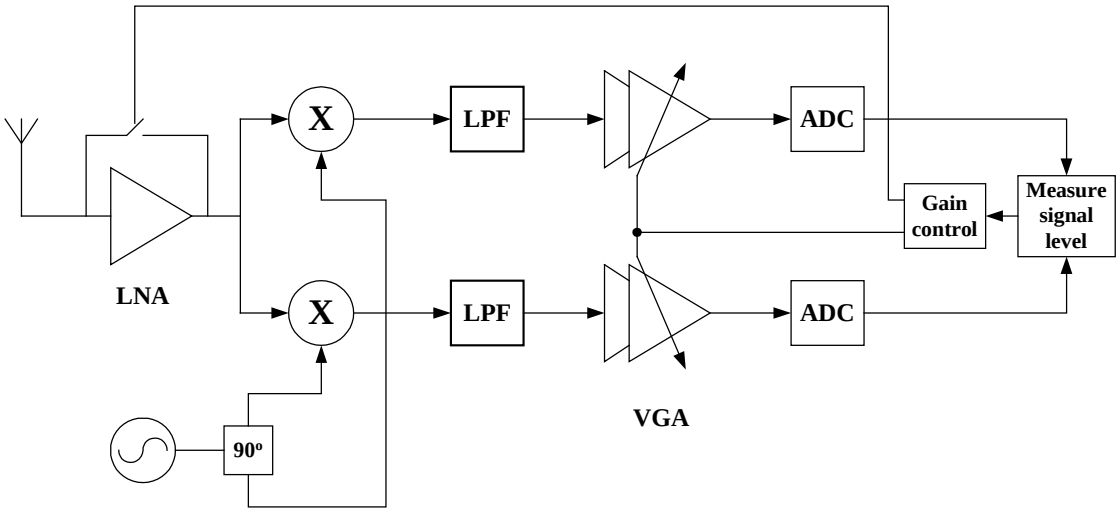
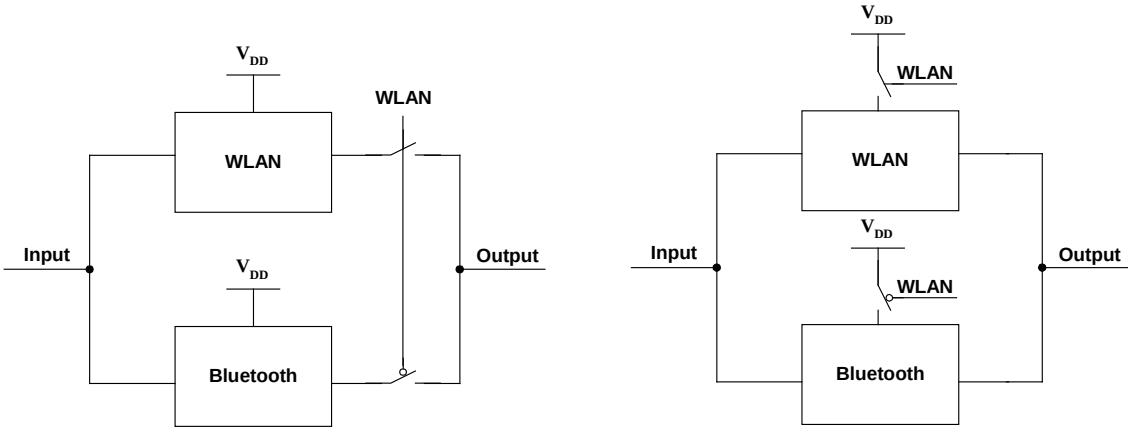


Fig. 3.1 Direct conversion receiver

3.2. Filter Specifications

The dual-mode filter can be implemented as two separate filters as shown in Fig. 3.2. Fig. 3.2(a) shows one possibility of having a common input to both filters and choosing one output according to the required standard. This solution suffers severely from nonlinearity of the switches since they are in the signal path. The other possibility is

shown in Fig. 3.2(b), where the input is also common to both filters but one filter is shut down according to the required standard. In this solution the nonlinearities of the switches does not deteriorate the overall linearity performance of the filter and thus it is adopted in this design.



(a) (b)

Fig. 3.2 Dual-mode filter (a) switch at the output (b) switch the power supply

It is even more challenging to share the same filter structure for both standards. Since the filter specifications are determined in order to comply with the standard, we have two different sets of specifications for each standard. The more stringent requirements should be met. The filter specifications for both standards are given in Table 3.1. The IEEE 802.11b standard attenuation requirements are more stringent. It specifies that the receiver should be able to handle an interferer at 25MHz with a power 35dB above the signal of interest and still keep the 10^{-5} BER performance. This test is done for a SNR

6dB above the minimum sensitivity level, i.e., a degradation of 6dB in the BER vs. SNR performance can be tolerated in the presence of the interferer.

Table 3.1 Filter specifications

Requirement	**Bluetooth**	**IEEE 802.11b**
Passband gain	6dB	6dB
Attenuation	45dB @ 3MHz	45dB @ 25MHz
Out-band IIP_3	20dBm	20dBm
NF	42dB	32dB
Current consumption	minimum	minimum
Power supply	2.5V	2.5V

There is a trade-off between the filter's cut-off frequency and the filter's order. Choosing a lower cut-off frequency will result in a lower order for the same attenuation at stopband. The drawback will be the deterioration in the demodulator performance (BER vs. SNR) since the baseband signal power can be affected. For the bluetooth signal 99% of the baseband signal power is contained within 430kHz. Simulation results show that a 4^{th} order Butterworth with a cut-off frequency f_c of 600kHz meets the attenuation requirements. The required SNR, to achieve the 0.1% BER required for the Bluetooth standard, with the filter included is around 13.5dB. Matlab simulation results also shows that a ±10% variations of the center frequency results in only 0.2dB increase in the required SNR. Since an odd order is required to add a single passive pole in order to

improve the out-of-band linearity, as will be discussed in section 4.1, a 5^{th} order Butterworth filter will be implemented. The filter's group delay variation is less than 0.5μS within the passband.

The same filter structure is also used for the IEEE 802.11b standard changing only the cut-off frequency. System level simulations were run to determine whether a 5^{th} order Butterworth baseband LPF with f_c=6MHz is sufficient to attenuate the interferer and comply with specifications for the IEEE 802.11b case. Note form Fig. 3.3 that the required SNR is about 12.5dB to comply with the 10^{-5} BER performance required by the standard. As it can be also observed from Fig. 3.3, the degradation for the case of an interferer at 25 MHz with a power 35dB above the signal of interest is about 3.5dB more

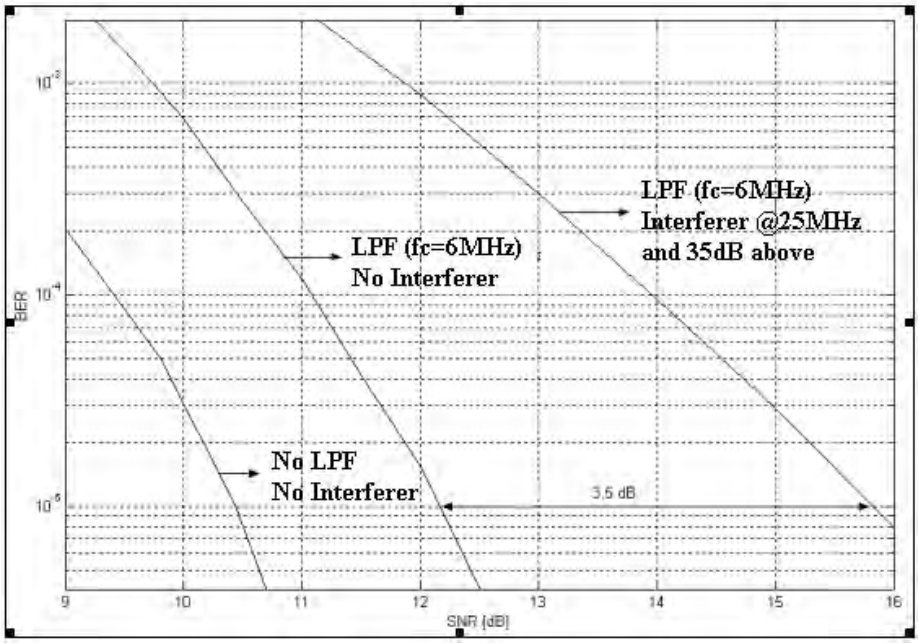


Fig. 3.3 Degradation in BER vs. SNR performance with baseband LPF and interferer

When the power of the interferer is swept while keeping a constant SNR of 16.5dB (that is 6dB more than required to obtain the specified BER in the ideal response), it is found that an interferer with a power up to 35.5dB above the signal level can be tolerated. This can be observed in Fig. 3.4(a).

The sensitivity of the receiver, however, will be determined by the required SNR to obtain the specified BER in the presence of the baseband LPF, that is, about 12.5dB. Fig. 3.4(b) shows the effect of sweeping the power of the interferer while keeping a constant SNR of 12.5+6 = 18.5dB. The results suggest that an interferer with a power up to 36.5dB can be tolerated.

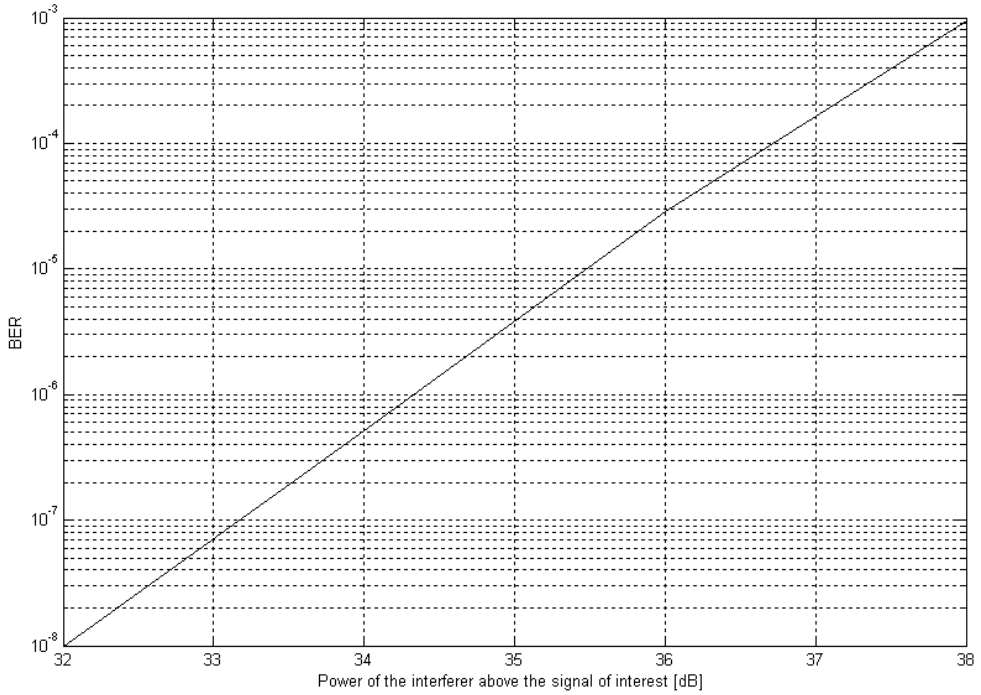


Fig. 3.4(a) Degradation in BER with increasing power in interferer (SNR=16.5dB)

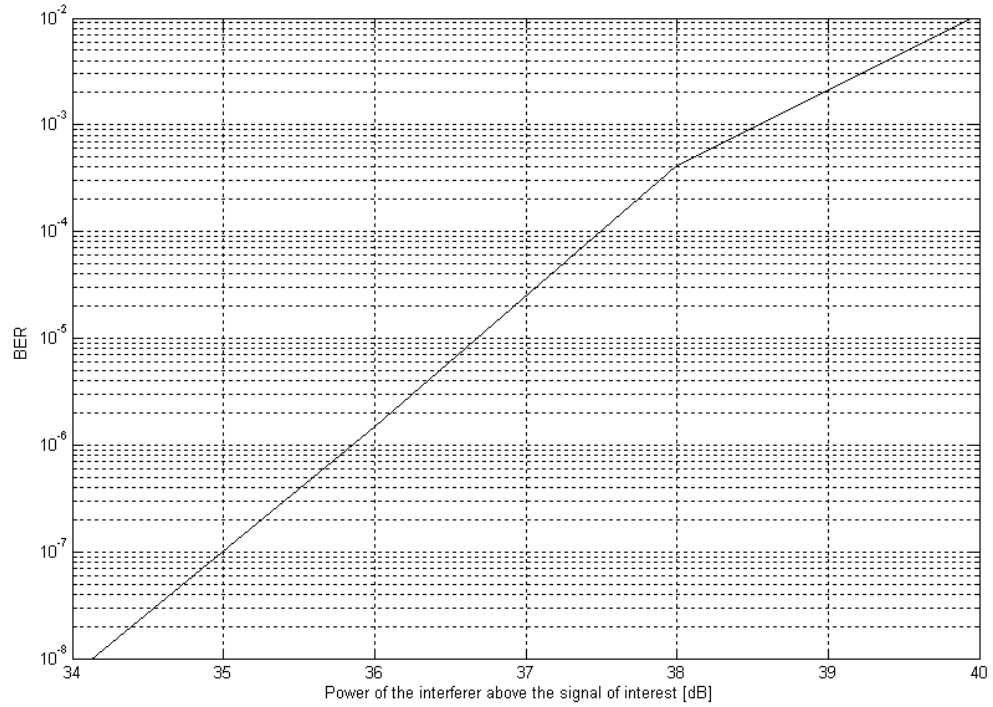


Fig. 3.4(b) Degradation in BER with increasing power in interferer (SNR=18.5dB)

3.3. Filter Architecture

The filter is implemented as an OTA-C filter with two cascaded biquadratic sections and a single passive pole as shown in Fig. 3.5 (a). A biquadratic section is shown in Fig. 3.5(b).

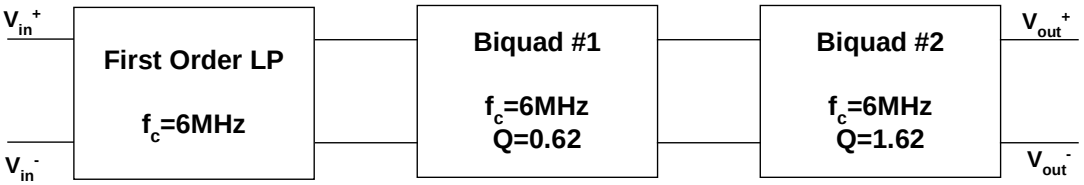


Fig. 3.5(a) Butterworth filter block diagram

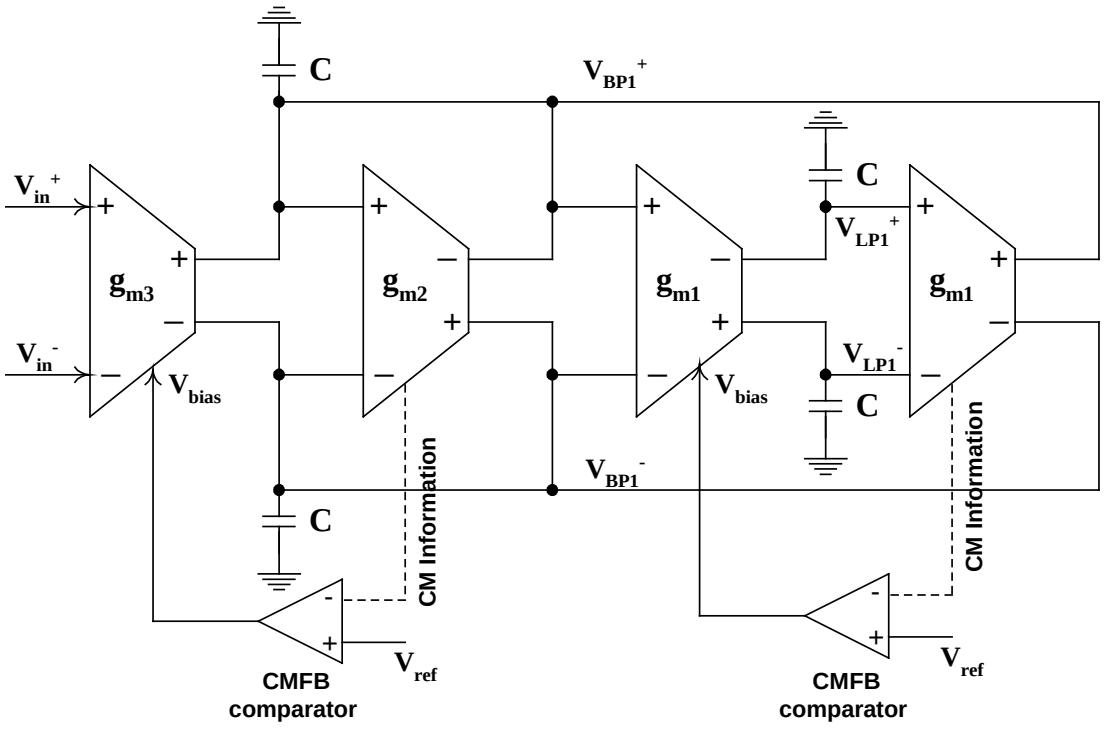


Fig. 3.5(b) Biquadratic section

It can be shown that the voltage transfer functions are given by:

$$\frac{V_{BP}}{V_{in}}(s) = \frac{\frac{g_{m3}}{C}s}{s^2 + \frac{g_{m2}}{C}s + \frac{g_{m1}{}^2}{C^2}} \tag{3.1}$$

$$\frac{V_{LP}}{V_{in}}(s) = \frac{\frac{g_{m3}.g_{m1}}{C^2}}{s^2 + \frac{g_{m2}}{C}s + \frac{g_{m1}{}^2}{C^2}} \tag{3.2}$$

where $\omega_0 = \frac{g_{m1}}{C}$, and $Q = \frac{g_{m1}}{g_{m2}}$

The OTA used is a source degenerated transconductance as shown in Fig. 3.6. Source degeneration is used to enhance the limited linear input range of a typical bipolar differential pair.

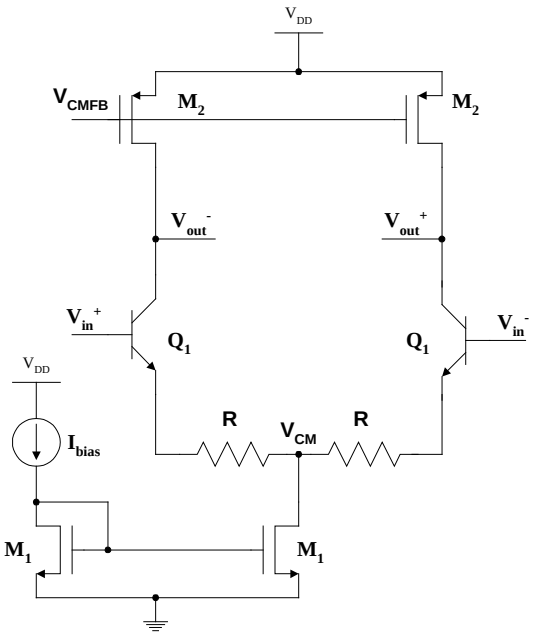


Fig. 3.6 Source degenerated OTA

3.4. Design Trade-offs

In this section different design considerations and trade-offs; linearity, noise, power consumption, and area are discussed.

3.4.1 Linearity Analysis

The voltage to current conversion relationship of the source degenerated OTA, shown in Fig. 3.6, can be written as:

$$\frac{i_{od}}{I_{bias}} = \tanh\left(\frac{v_d}{2V_t(1+g_{m1}R)}\right) \tag{3.3}$$

where $\tanh x = x - \frac{x^3}{3} + ...$

Thus we can write $i_{od} = a_0 + a_1 v_d + a_2 v_d^2 + a_3 v_d^3 + ...$

Using Taylor series expansion of equation (3.3) , we get:

$$i_{od} = \frac{I_{bias}}{2V_t(1+g_{m1}R)} v_d - \frac{1}{3}\frac{I_{bias}}{(2V_t)^3(1+g_{m1}R)^3} v_d^3 \tag{3.4}$$

$$a_0 = a_2 = 0,\ a_1 = \frac{I_{bias}}{(2V_t)(1+g_{m1}R)} = G_m, \text{ and } a_3 = \frac{1}{3}\frac{I_{bias}}{(2V_t)^3(1+g_{m1}R)^3} \tag{3.5}$$

For $v_d = A \times \cos \omega t$, the following expressions for the third harmonic distortion and the second harmonic distortion (assuming ε% of mismatches) can be obtained as discussed in Appendix A to be:

$$HD_3 = \frac{1}{12}\frac{A^2}{(2V_t)^2(1+g_{m1}R)^2} \tag{3.6a}$$

$$HD_2 = \varepsilon\frac{1}{4}\frac{A}{(2V_t)(1+g_{m1}R)} \tag{3.6b}$$

The third intermodulation distrotion (see Appendix A) can be obtained as:

$$IIP_3 = \sqrt{\frac{4}{3}\frac{a_1}{a_3}} = \frac{A}{\sqrt{IM_3}} \Rightarrow IIP_3(dB) = A_{dB} - \frac{1}{2}IM_{3dB} \tag{3.7a}$$

$$IIP_3 = 4V_t(1+g_{m1}R) \cong 2I_{bias}R \tag{3.7b}$$

The minimum power supply voltage V_{DD_min} and the common mode range (CMR) are given by:

$$V_{DD\_\min} = V_{dsat2} + V_{CE\_ON} + 0.5I_{bias}R + V_{dsat1} \tag{3.8a}$$

$$0.5I_{bias}R + V_{dsat1} + V_{BE\_ON} < CMR < V_{DD} - V_{dsat2} + V_{BE\_ON} \tag{3.8b}$$

$$V_{dsat2} = \sqrt{I_{bias} / \mu_P C_{OX} (W/L)_2} \tag{3.8c}$$

where $V_{BE\_ON} \cong 0.8V$, and $V_{CE\_ON} \cong 0.3V$. As an example for I_{bias}=0.1mA, R=4kΩ, V_{dsat1}= V_{dsat2}=0.5V. The value of V_{DD_min} is 1.5V, and 1.5V<CMR<1.8V.

Frequency Response. Considering the OTA of Fig.3.6, it can be shown that:

$$g_m(s) = \frac{i_{od}}{v_d}(s) \cong \frac{(g_{m1} - sC_{BC})(1 + sC_E R)}{(1 + g_{m1}R + sC_E R)} = \frac{g_{m1}}{1 + g_{m1}R} \frac{(1 - s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{nd})} \tag{3.9a}$$

where C_{BC} is the parasitic capacitance between the base and collector of Q_1, and C_E is the parasitic capacitance between the emitter and ground.

The excess phase $\Delta\phi$ can be expressed as:

$$\Delta\phi = -\tan^{-1}(\omega/\omega_{z1}) + \tan^{-1}(\omega/\omega_{z2}) - \tan^{-1}(\omega/\omega_{nd}) \tag{3.9b}$$

where $\omega_{z1} = \frac{g_{m1}}{C_{BC}}$, $\omega_{z2} = \frac{1}{RC_E}$, and $\omega_{nd} = \frac{1 + g_{m1}R}{RC_E}$

3.4.2 Effect of the Single Passive Pole

To improve the out-of-band linearity, a first order passive pole is used at the input stage of the filter. This improvement is due to the attenuation of the undesired interferes. This also has the benefit of increasing the attenuation of the filter, i.e., increasing the

filter order by 1. This is done at no cost in power. The cost is rather in area and noise. From simulation results, adding the first order pole improves the out-of-band IIP_3 by about 10dB and deteriorate the NF by about 1.5dB, i.e., an improvement in the SFDR by about 5.67dB.

Lack of tracking between the single pole resistors and the transconductances of the G_m cells, would result in passband ripple. Thanks to the chosen topology of the source degenerated OTA where the transconductance of the G_m cell is related to the source degeneration resistor as given by equation (3.10):

$$G_m = \frac{1}{R} \times \frac{g_{m1}R}{1+g_{m1}R} = \frac{1}{R} \times \frac{n}{1+n} \tag{3.10}$$

Variations in the factor n of x% due to process drifts result in variations of x/(1+n+nx) for the factor (n/1+n). Thus although the variations in factor n may be as large as 50%, the variations in the factor (n/1+n) will be only about 3% for n=10. It has been verified from simulations that this ripple is around 0.2dB which is acceptable for the current application.

Since the out-of-band blockers will be attenuated by the filter, harmonics generated by the out-of-band blockers are dominated by the filter's first stage. Hence, to improve the overall filter linearity, the first stage is designed to have better linearity by using more current I_{bias}. Increasing the current of the first stage by 50% (the total current by 10%) results in a 3dB improvement in IIP_3 of the overall filter. This would be otherwise obtained by doubling the total current consumption.

3.4.3 Noise Analysis

The input referred noise spectral density can be calculated as:

$$\begin{aligned} v_{ieq}^2 &= \frac{4KT}{RG_m^2} + \frac{8KTg_{m2}}{3G_m^2} + \frac{kg_{m2}^2}{W_2L_2C_{OX}fG_m^2} + 4KT\left(r_b + \frac{1}{2g_{m1}}\right) \\ &= 4KTR\left(1+\frac{1}{g_{m1}R}\right)^2 + \frac{8KT}{3}g_{m2}R^2\left(1+\frac{1}{g_{m1}R}\right)^2 \\ &\quad + \frac{k}{W_2L_2C_{OX}f}(g_{m2}R)^2\left(1+\frac{1}{g_{m1}R}\right)^2 + 4KT\left(r_b + \frac{1}{2g_{m1}}\right) \end{aligned} \tag{3.11}$$

For $g_{m1}R >> 1$,i.e., for high linearity, equation (3.11) can be approximated as:

$$v_{ieq}^2 = 4KTR\left(1+\frac{2}{3}g_{m2}R\right) + \frac{k}{W_2L_2C_{OX}f}(g_{m2}R)^2 \tag{3.12}$$

Equation (3.12) shows that effect of the source degeneration on the noise performance of the OTA is almost negligible.

An expression for the SNR can be obtained using equations (3.7b) and (3.12), neglecting flicker noise, as follows:

$$SNR = \frac{I_{bias}}{2KT(3+2g_{m2}R).BW} \tag{3.13}$$

where BW is the equivalent noise bandwidth.

Note in equation (3.13) and Fig. 3.7 (for BW=6MHz, and R=4kΩ) that increasing the current I_{bias} improves the SNR. This is a clear SNR-power consumption trade-off. In order to reduce the noise contribution of the current sources M_2, g_{m2} should be minimized. Since I_{bias} is determined based on the linearity requirement, g_{m2} can be reduced by reducing $(W/L)_2$ which would increase V_{dsat2} and the performance become limited by the power supply.

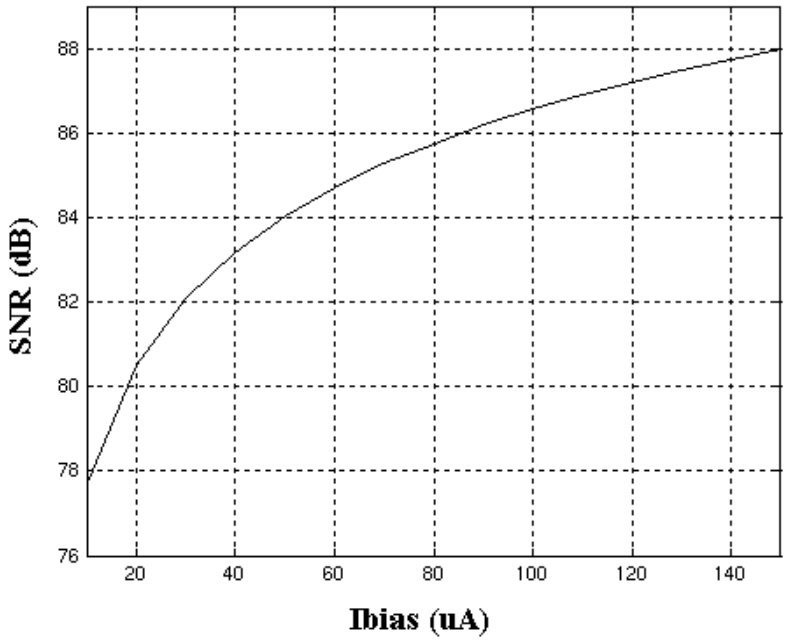


Fig. 3.7 SNR vs. Ibias

For the case of Bluetooth, where the filter bandwidth is close to the flicker noise corner, the noise performance will be dominated by the flicker noise of M_2. The transistor length L_2 should be selected large enough to achieve the required noise performance. To be able to meet the noise requirement on the filter, all the required gain (6dB) is placed at the first biquadratic section. This will optimize the noise performance and the price is the degradation in the in-band linearity performance.

3.4.4 Input Impedance

The input impedance is given by:

$$Z_{in} = r_{\pi} + (\beta + 1)R = \frac{\beta}{g_{m1}} + (\beta + 1)R \cong \beta R \qquad (3.14a)$$

Thus there is a trade-off in, as shown in Fig. 3.8, choosing between the noise performance and the input impedance. Choosing a larger resistor value will improve the input impedance but will increase noise at the same time.

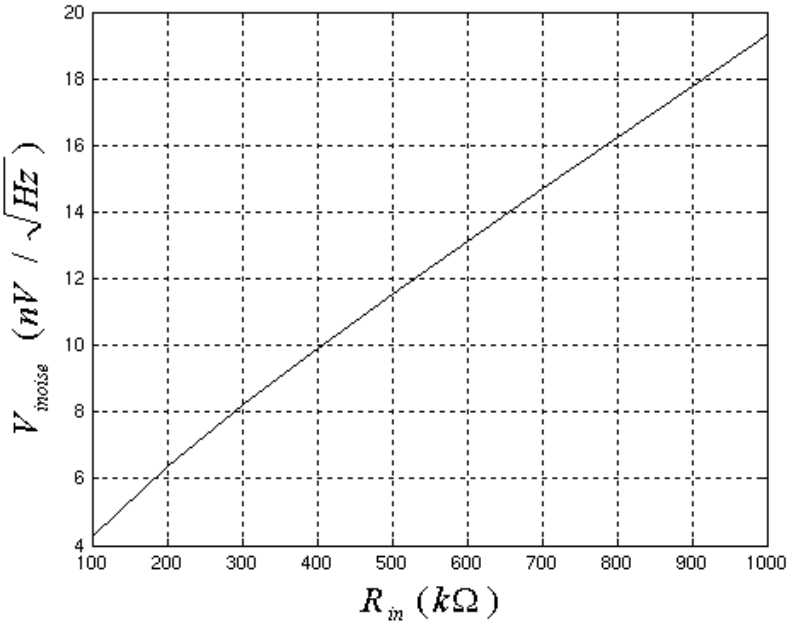


Fig. 3.8 $V_{in,noise}$ vs. R_{in}

3.4.5 Output Impedance

The input impedance is calculated:

$$Z_{out} = (1 + g_{m1}R)r_{0Q} \,//\, r_{02} \cong g_{m1}R \times r_{0Q} \,//\, r_{02} \cong \frac{V_A}{V_t} R \,//\, r_{02} \qquad (3.14b)$$

Since L_2 is chosen to be large to reduce the flicker noise. For example, choosing L_2=6μm results in r_{02} of 2MΩ. This results in an output resistance of 333kΩ, for $V_A/V_t \cong 100$ and R=4kΩ.

3.4.6 Design Procedure

Fig. 3.9 shows a flow chart that contains a design procedure for the OTA.

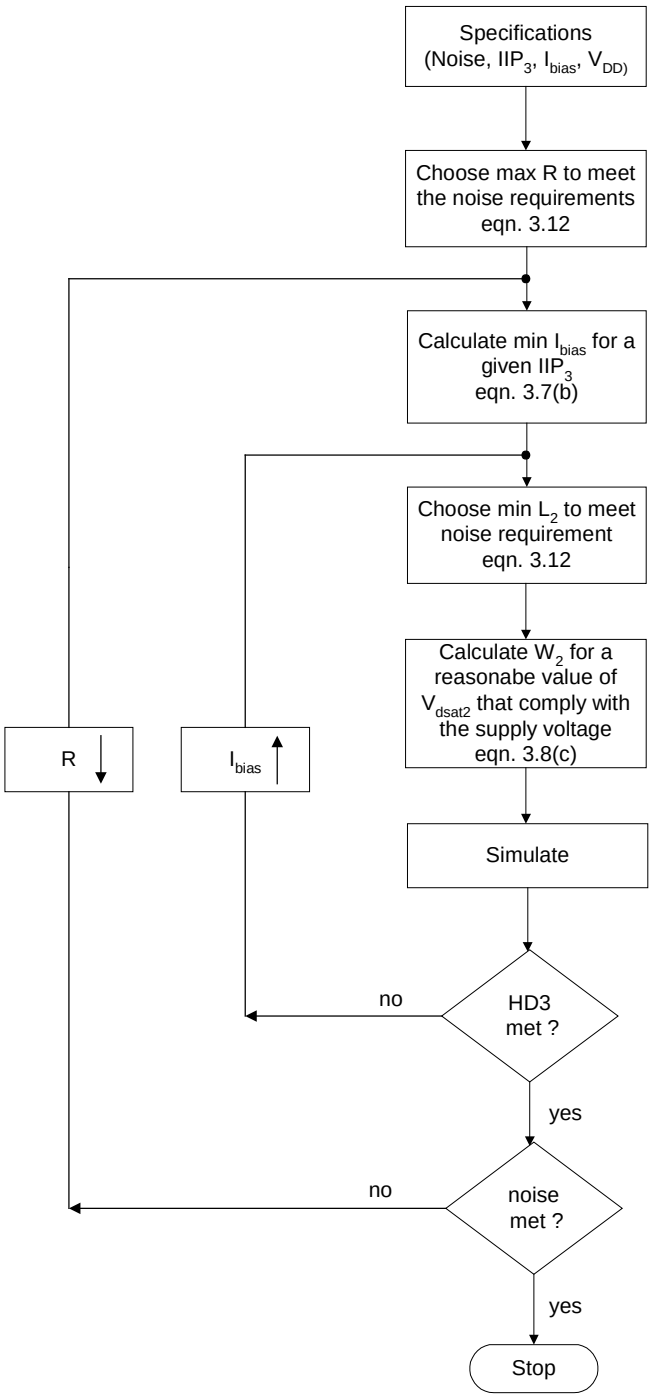


Fig. 3.9 Design procedure flow chart

Design Example. The design example assumes IBM 0.25μm BiCMOS process. In the first example, the design goals are NF of 42dB, IIP_3 of 0dB, and minimum power consumption with a supply voltage of 2.5V. A NF of 42dB corresponds to an input referred noise of 11.3nV/√Hz. According to equation (3.12), the maximum value of the resistance to meet this requirement is 4.7kΩ assuming $g_{m2}R \cong 1$. Thus R is chosen to be 4kΩ. According to equation (3.7b) and for IIP_3 of 0dB (a value of 1), the minimum I_{bias} is calculated to be 125μA. L_2 is chosen to be 6μm to reduce the flicker noise. $(W/L)_2$ is chosen as the minimum value in order to comply with the supply voltage, i.e., a reasonable value for V_{dast2}. For V_{dsat2}=0.5V, $(W/L)_2$ can be calculated to be 7, i.e, W_2=42μm for L_2=6μm.

3.5. OTA Architecture

The proposed OTA architecture for the dual-mode filter is shown in Fig. 3.10. The OTA is based on the well-known source degeneration configuration with current scaling, as shown in Fig. 3.10(a). Note that due to the very different requirements of bandwidth of both standards the power consumption is not optimal if the same current is used in both standards. In particular, Bluetooth needs less current to achieve almost same linearity as IEEE 802.11b [see equation (3.9)]. This makes the proposed OTA architecture unique in terms of current scaling. The bias current is scaled with the same factor as the resistance to keep the product $I_{bias} \times R$, or equivalently the linearity, constant for both standards. The active loads M_2 are also scaled accordingly by increasing the

width of the load transistors (by switching in $4M_2$) so as to keep the source-gate voltage constant in the two modes.

The element that is chosen to be switched to choose between the two standards is the source degenerated resistor. To avoid wide spread of the resistor values (ten times difference in the cut-off frequency of both standards), the integrating capacitors can be switched simultaneously. Fig. 3.10(b) shows a resistor value scaling of 5 and doubling the capacitance to achieve a scaling factor 10 in the cut-off frequency.

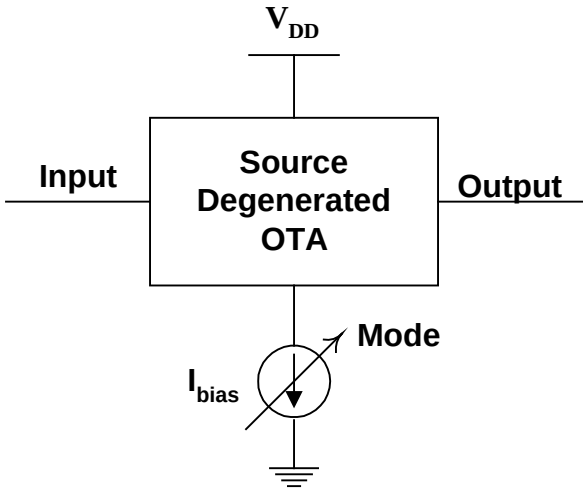


Fig. 3.10(a) Conceptual block diagram of the proposed OTA

The dimensions of the switches in series with the degeneration resistors is chosen to make the switch resistance about 1% of the resistor such that the linearity performance of the OTA, and consequently the filter, is almost not affected.

Table 3.2 summarizes the values of the transistors' dimensions, resistors and capacitors used in the designed OTA.

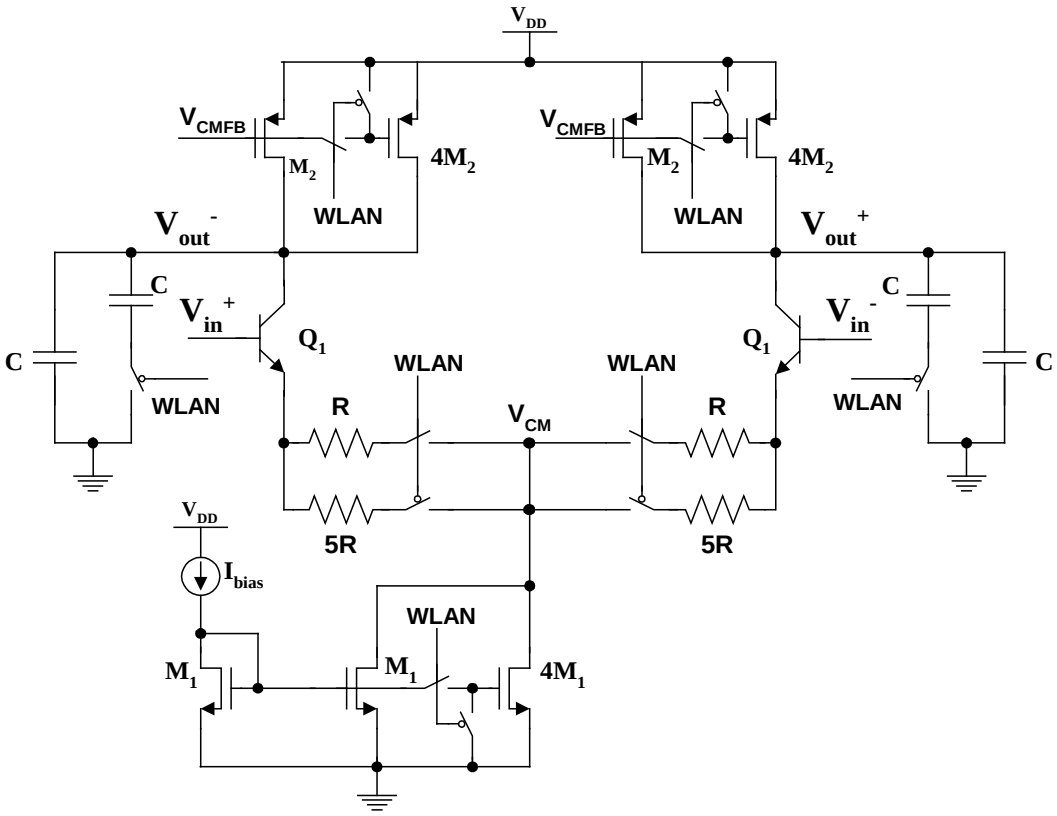


Fig. 3.10(b) Circuit implementation of the dual standard OTA

Table 3.2 Dimensions of the designed OTA

M_1	8µ/1.2µ	**M_2**	9.6µ/6µ
Q_1	0.44µ×3µ×1	**R**	4kΩ
C	5.65pF	**M_{switch}**	40µ/0.24µ

3.6. Common-mode Feedback

Direct connection between consecutive OTAs in the filter is exploited in the implementation of the CMFB circuit as shown in Fig. 3.5(b) and Fig. 3.11 (CMFB comparator). The implementation of a separate common-mode detector is avoided since

the common mode information is extracted at V_{CM}. This voltage is shifted up by transistor M_S to be within the input common mode range of the comparator, composed of the differential pair transistors M_A and diode connected transistors M_2, which compares V_{CM} and V_{ref} and fix the output DC CM voltage accordingly. In this design the DC voltage is chosen to be about 1.6V. The expression of V_{CM} of the common-mode detector has been shown in Table 2.2 of section 2.1.2.

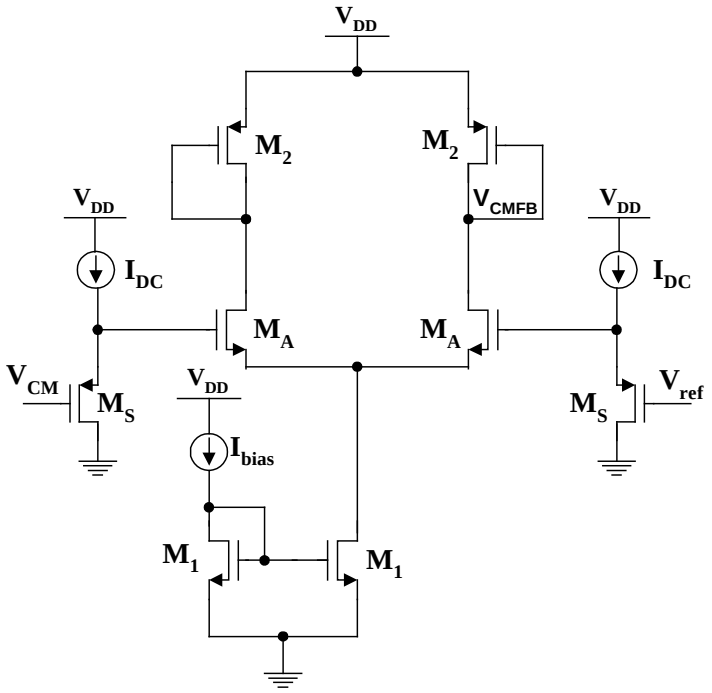


Fig. 3.11 CMFB comparator

3.7. Simulation Results

The filter has been simulated for both modes. Table 3.3 summarizes the simulated filter performance parameters for both operational modes.

Table 3.3 Summary of performance

	Bluetooth filter	**WLAN filter**
Filter type	Butterworth	Butterworth
Filter order	5	5
Cut-off frequency	600kHz	6MHz
IIP_3	40dBm [1]	45dBm [2]
Integrated input referred noise	$90\mu V_{rms}$	$100\mu V_{rms}$
Power supply	2.5V	2.5V
Current consumption [4]	1mA [3]	3mA [3]
Area (estimated) [4]	$0.9mm^2$	$0.9mm^2$

[1] Two tones applied at 1.83MHz and 3.16MHz
[2] Two tones applied at 18.3MHz and 31.6MHz
[3] Including CMFB and biasing circuitry
[4] I and Q branches

Fig. 3.12(a) and Fig. 3.13 shows the magnitude response for the IEEE 802.11b and Bluetooth filter modes, respectively. The phase response for the IEEE 802.11b filter is shown in Fig. 3.12(b). Fig. 3.14 shows the output noise spectral density for the IEEE 802.11b filter mode to be about 60.7nV/√Hz. The result of the two-tone intermodulation test for the IEEE 802.11b is shown in Fig. 3.15. The two tones are applied at 1.83MHz and 3.16MHz such that their third order intermodulation cross product (at 5MHz) falls inside the pass band of the filter.

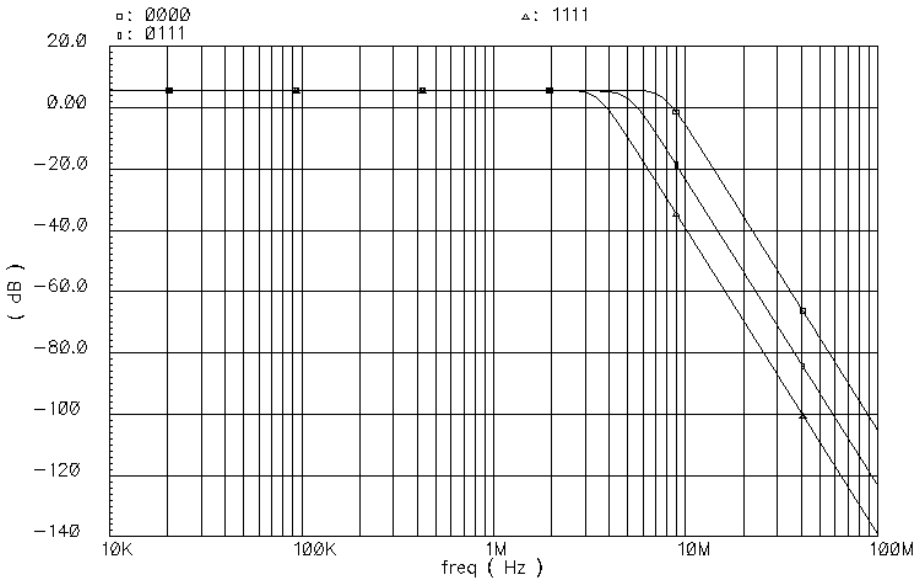


Fig. 3.12(a) Magnitude response for the IEEE 802.11b filter mode

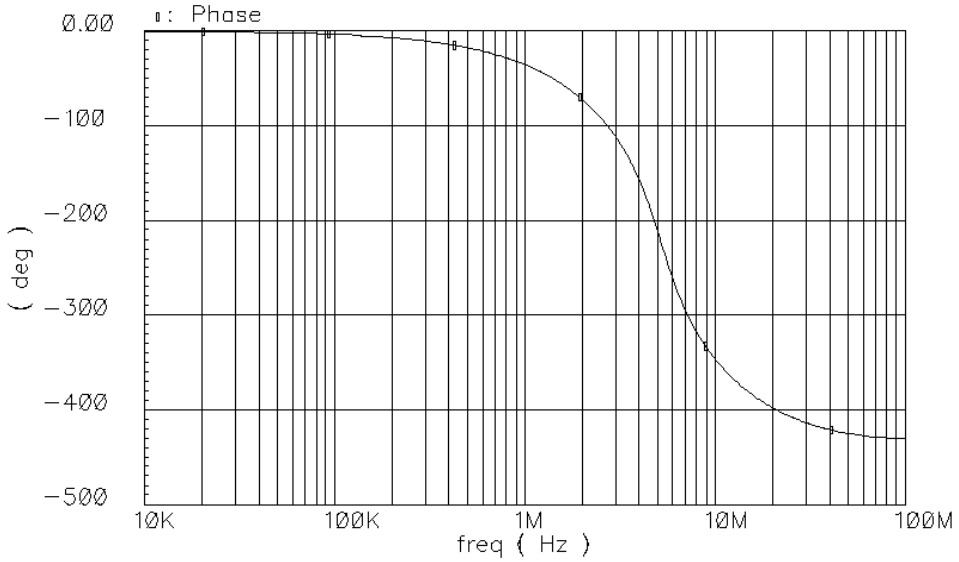


Fig. 3.12(b) Phase response for the IEEE 802.11b filter mode

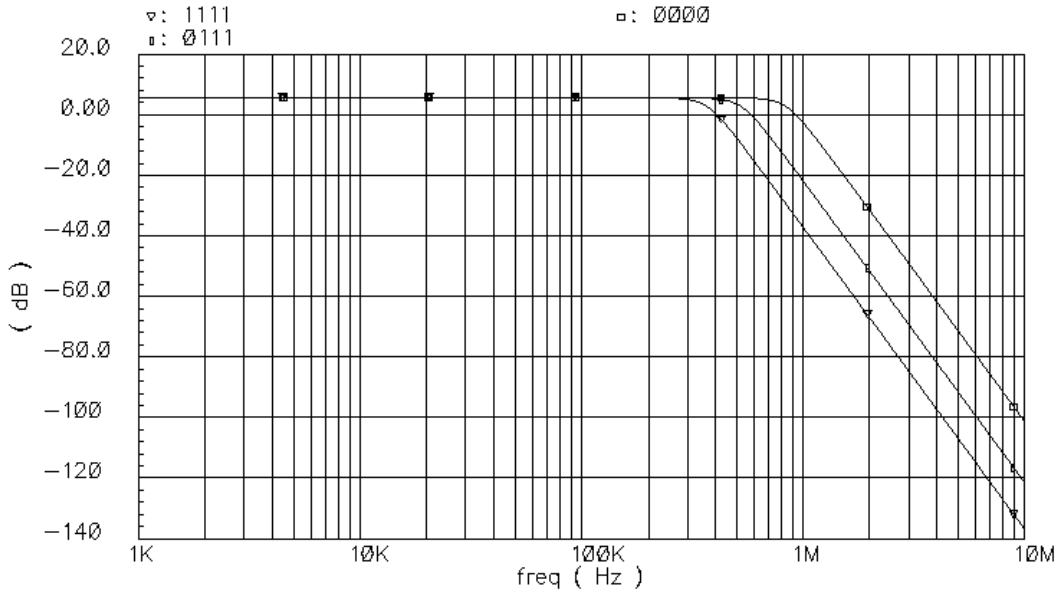


Fig. 3.13 Magnitude response for the Bluetooth filter mode

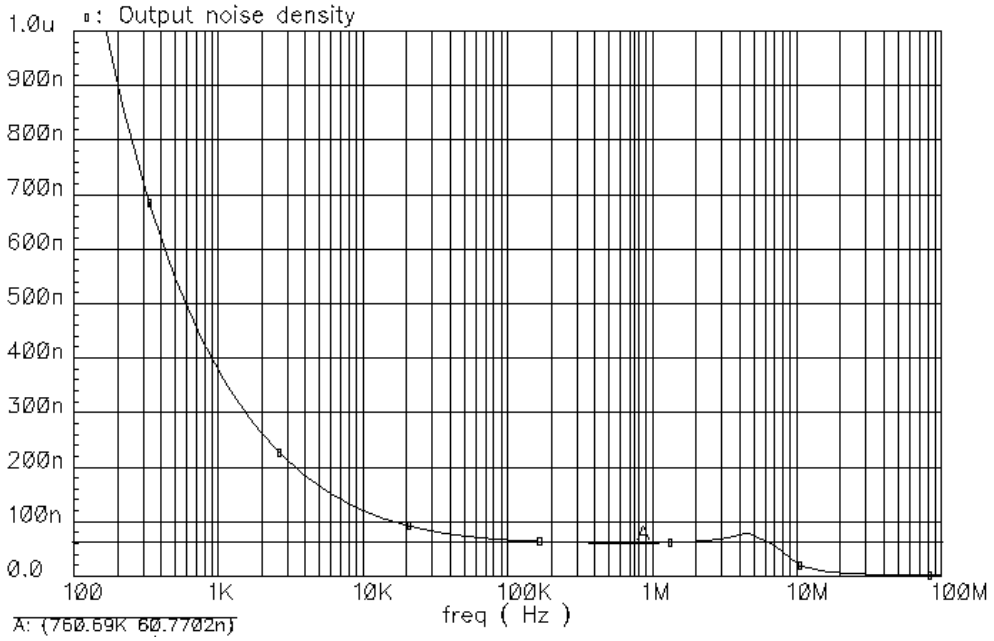


Fig. 3.14 Output noise spectral density for the IEEE 802.11b filter mode

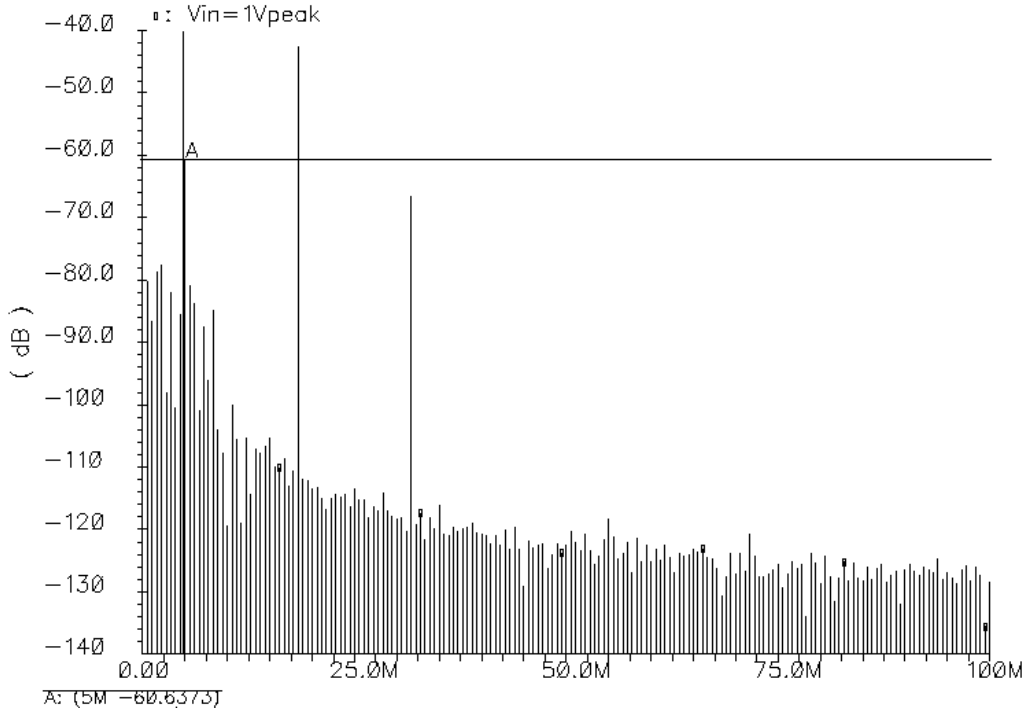


Fig. 3.15 Two tone intermodulation test for IEEE 802.11b filter mode

Table 3.4 contains comparison with the latest designs reported in the literature [47,53-57]. The figure of merit (FoM) [57] is defined in equation (3.15).

$$FoM = \frac{Power\ dissipation}{(\#of\ \ poles)\times(cutoff\ \ frequency)\times SFDR} \tag{3.15}$$

$$SFDR = \frac{1}{1.5}\left(IIP_3 + 174dBm - 10\log B - NF\right) - SNR_{\min} \tag{3.16}$$

where SNR_{min}=3dB.

For example, for the IEEE 802.11b the noise bandwidth B=6MHz. For an out-of-band IIP_3 of 45dB and a NF of 32dB, the out-of-band SFDR can be calculated from (3.16) to be 76dB, which results in a FoM=3×10^{-18}J.

Table 3.4 Comparison with recently published work

	[47]	**[53]**	**[54]**	**[55]**	**[56]**	**[57]**	**This Work**
Approximation	Chebyschev	Elliptic	Butterworth	Chebyschev	Butterworth	Elliptic	Butterworth
Order	4	7	5	5	6	5	5
Topology	OTA-C	OTA-C	OpAmp-RC	OpAmp-RC	CF-RC	MOSFET-C	OTA-C
Cutoff frequency (MHz)	0.2	0.63	2	2	2	2	6
Passband gain (dB)	10	31	18	20-68	18	9	6
In-band IIP_3 (dB)	14	20	-	9	22	11	12
Out-band IIP_3 (dB)	49	30	48	38	51	41	45
NF (dB)	30	36	32	21	37	32	32
Input referred noise (nV/√Hz)	28	55	33	9.4	60	33	33
Out-band SFDR (dB)	90	70	82	82	80	77	76
Power supply (V)	2.7	3	2.7	2.7	2.7	2.7	2.5
Current drain (mA)	11.5	16	4.7	4.3	2.25	2.3	1.5
Power/pole (mW)	7.76	6.86	2.54	2.32	1.01	1.24	0.75
Area (mm^2)	1.2	5	2.4	1.35	1.25	2.8	1.5
Technology (μm)	0.8 BiCMOS	1.2 CMOS	0.35 BiCMOS	0.35 BiCMOS	0.5 CMOS	0.8 BiCMOS	0.25 BiCMOS
FoM (J)	38.8×10^{-18}	10.8×10^{-16}	8×10^{-18}	7.4×10^{-18}	5.1×10^{-18}	12.4×10^{-18}	3×10^{-18}
Relative FoM	5.2	146	2.7	2.5	1.7	4.1	1
On-chip tuning	OTA	5-bit C array	5-bit C array	5-bit C array	No	MOS R	4-bit C array

3.8. Frequency Tuning Scheme

The implemented frequency tuning strategy depends on implementing the integrating capacitors as a bank of unit capacitors, i.e., a programmable capacitor array (PCA). This solution has been chosen rather than tuning the transconductors, using a control voltage, since it is optimum for dynamic range and power consumption. The implemented solution does not involve changing the dynamic range of the filter since the bias conditions of the OTA and thus linearity of the filter is unchanged during tuning. The cost is more area due to switches and control circuitry of the PCA. The number of bits in the capacitor bank is determined according to the required accuracy. The maximum quantization error ε_{max} in an N-bit capacitor array with a ±x% range to be covered is given by equation (3.17).

$$\varepsilon_{\max} = \pm \frac{1}{2^N} \frac{x}{100 - x} \tag{3.17}$$

The required accuracy in the tuning system is ±10%, according to the system level simulations discussed in section 3.2. For x=40% and choosing N=4 results in ε_{max} = ±4.2%, which gives some extra room for other sources of error in the tuning scheme such as: mismatches and the limited precision of the tuning control loop itself.

Using a conventional tuning circuit based on PLL is not suitable for filters with PCAs [22]. The output of the filter in the PLL is an analog voltage, which cannot be interfaced directly with the PCAs and an additional A/D interface is needed, as shown in Fig. 3.16. An XOR gate is used as the phase comparator and the master oscillator used is a relaxation oscillator.

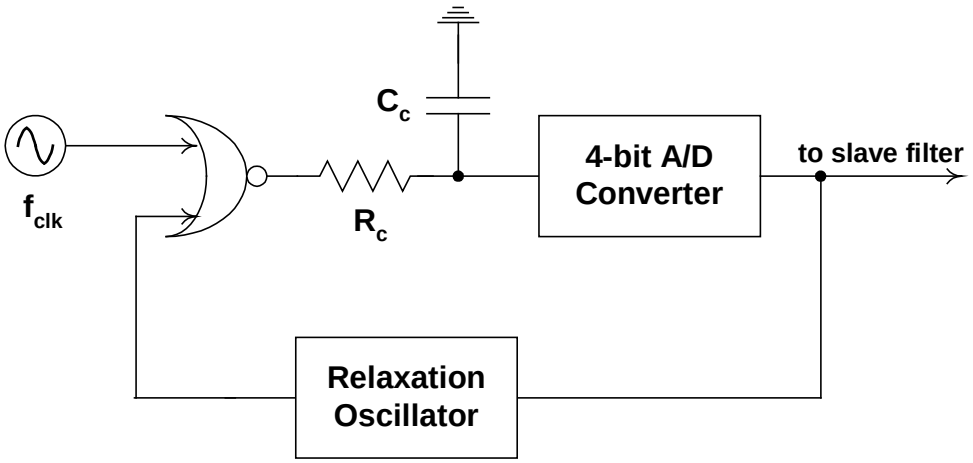


Fig. 3.16 Frequency tuning scheme based on a VCO

On the other hand, the implemented automatic frequency tuning scheme, shown in Fig. 3.17, lends itself natural to filters with PCAs. The output of the counter is directly connected to the switches of the PCA in both the salve filter and the relaxation oscillator.

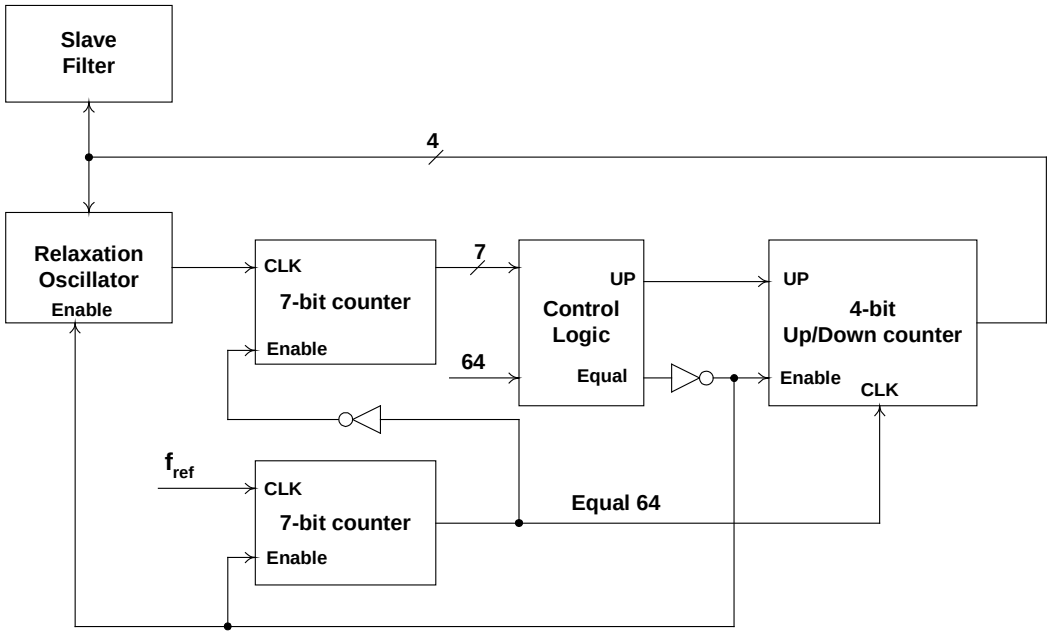


Fig. 3.17 Automatic frequency tuning scheme

The automatic tuning scheme consists of a master oscillator, one 4-bit up/down counter, two 7-bit counters, and the control logic. The 4-bit counter controls the 4-bit capacitor bank of the master oscillator and the slave filter. At the system reset, the 7-bit counters are reset to zero and the 4-bit counter is reset to the middle code 0111. The 7-bit counter connected to the reference frequency f_{ref} counts until it reaches 64, at that time the control logic disables the 7-bit counter connected to the master oscillator. The control logic then compares the contents of the 7-bit counter connected to the master oscillator with 64. The result of this comparison determines the direction that the 4-bit up/down counter will proceed.

If the number in the counter is between 60 and 68, the control logic sends a freezing signal which disables all the counters and switch off the master oscillator. The tuning is considered completed and the tuning bits are the contents of the 4-bit up/down counter. If the number in the counter is less than 60, which means that the master oscillator is counting slowly and some capacitance in the capacitor bank needs to be disconnected.

Thus, the control logic sends a down signal to the 4-bit up/down counter. At the time the 7-bit counter connected to f_{ref} reaches 128, a new tuning cycle starts. If the number in the counter is greater than 68, which means that the master oscillator is counting fast and some capacitance in the capacitor bank needs to be connected. Thus, the control logic sends an up signal to the 4-bit up/down counter. At the time the 7-bit counter connected to f_{ref} reaches 128, a new tuning cycle starts. The tuning will continue until a freeze signal, from the control logic, is detected.

The master oscillator is implemented as a relaxation oscillator as shown in Fig. 3.18. At the system reset, The S-R latch is reset to zero. This will cause M_1 and M_4 to be on and M_2 and M_3 to be off. This will result in V_{out}^- to be clamped at V_{DD}, while the voltage V_{out}^+ is changing with a constant negative slope ($g_m \times V_{bias}/C$) because the current I_{out} is flowing through M_1. The nominal value of the main capacitor is 6pF. Thus a parasitic capacitance of about 0.2pF and 30% mismatch between the parasitic capacitances in the relaxation oscillator and the slave filter, will result in 1% error, which will not affect significantly the accuracy of the frequency tuning.

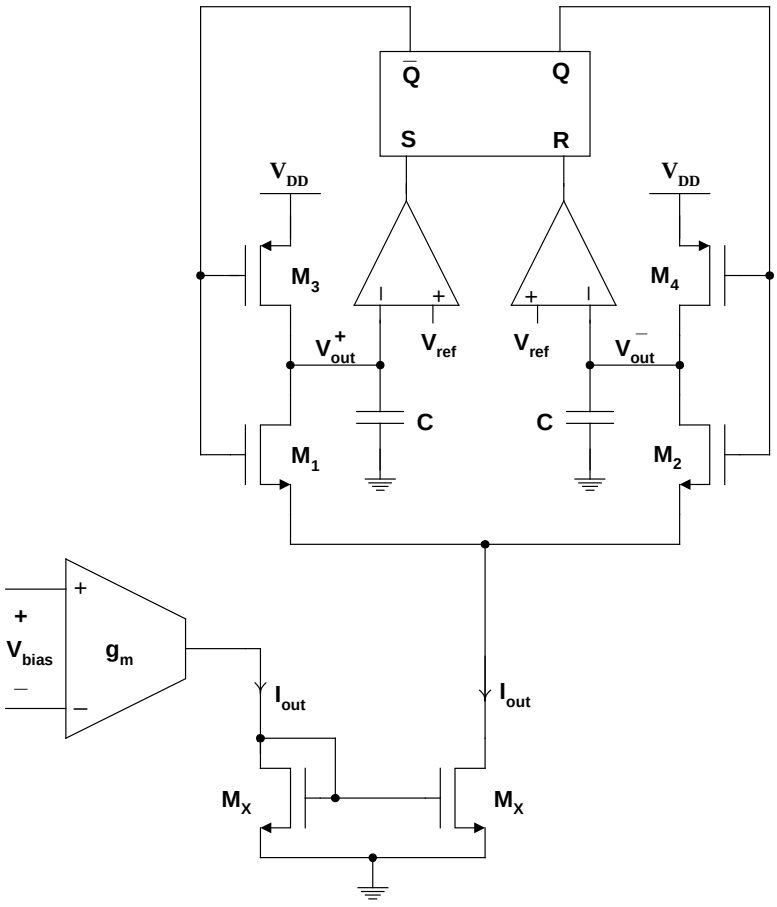


Fig. 3.18 Relaxation oscillator

When V_{out}^{+} reaches V_{ref}, after one-half of a clock period, the output of the corresponding comparator goes positive, which causes the S-R latch to become set. This causes M_2 and M_3 to turn on and M_1 and M_4 to turn off. When M_3 turns on, the voltage V_{out}^{+} is charged to V_{DD}. This causes the output of the corresponding comparator to go low, so both inputs to the S-R latch are again low. At the same time, since M_2 turns on, V_{out}^{-} becomes to decrease linearly until it reaches V_{ref}. This completes one period of oscillation.

After V_{out}^{-} reaches V_{ref}, the S-R latch is reset, V_{out}^{-} is charged to V_{DD} and V_{out}^{+} starts to discharge again. The outputs of the relaxation oscillator V_{out}^{+} and V_Q are shown in Fig. 3.19. The period of oscillation T_{osc} can be expressed as:

$$T_{osc} = \frac{2C}{g_m}\frac{V_{DD} - V_{ref}}{V_{bias}} \tag{3.18}$$

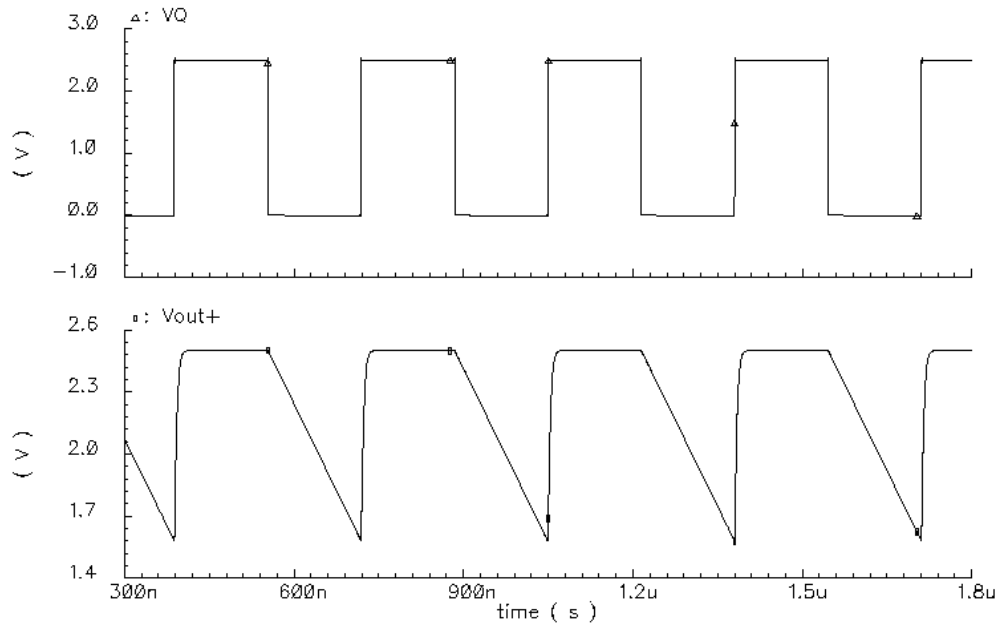


Fig. 3.19 Outputs of the relaxation oscillator

The voltages V_{ref} and V_{bias} should be obtained from a resistive string such that the ratio (V_{DD}-V_{ref}/V_{bias}) is independent of temperature and process variations. It can be predetermined with good accuracy depending on matching of the resistors. Hence, the oscillation frequency $f_{osc}(=1/T_{osc})$ is proportional to g_m/C. The feedback tuning loop ensures that the value of g_m/C (which is the cut-off frequency of the salve filter at the same time) remains constant in the presence of temperature and process drifts.

The tuning circuit (including the relaxation oscillator) occupies and area of $0.3mm^2$, as shown in the chip layout in Fig. 3.20. It dissipates a total current of 700μA. The same relaxation oscillator can be used in the PLL tuning scheme of Fig. 3.16. The phase comparator can be implemented as an XOR gate. The main area consumer in this scheme is the low-pass filter. The cut-off frequency of this low-pass filter should be chosen small enough since the DC component is the only component of interest from the output of the XOR gate. The cut-off frequency of the Bluetooth filter is 600kHz, thus the cut-off frequency of the PLL low-pass filter is chosen to be 100kHz. A 4-bit flash A/D converter can be used, with 16 resistors and 16 comparators, to provide the digital input to the slave filter. The value of the resistance used in the resistive string of the A/D converter is chosen as a trade-off between area and power consumption. A large resistor value will result in a large area A/D with low power consumption and vice versa. A value of 10kΩ is a good compromise. Table 3.5 shows a comparison of the PLL and digital tuning schemes. The PLL scheme consumes more area. Although the digital scheme consumes more power, but this is irrelevenat in this design since the digital logic and the relaxation oscillator are freezed after the filter is tuned.

Table 3.5 Comparison of PLL and digital tuning schemes

	PLL tuning scheme Fig. 3.16	**Digital tuning scheme Fig. 3.17**
Area	$0.5mm^2$	$0.3mm^2$
Current consumption	500μA	700μA

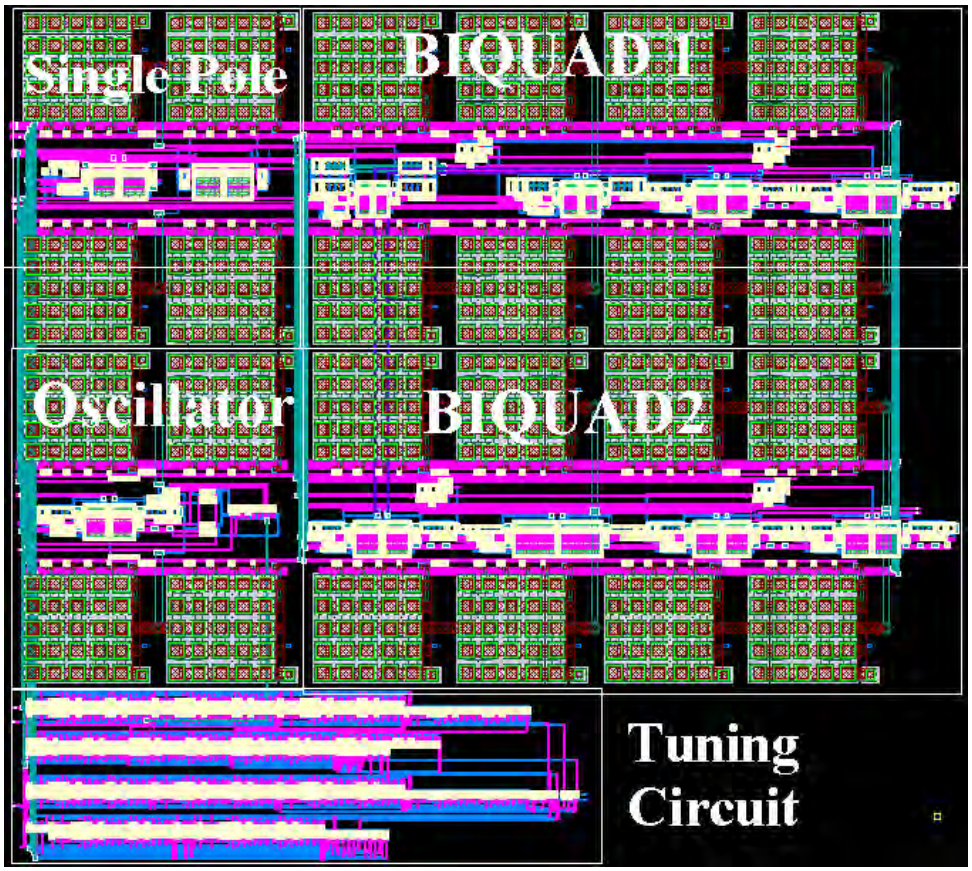


Fig. 3.20 Chip layout

CHAPTER IV

A 2.7V, 1.8GHZ, 4TH ORDER TUNABLE LC BANDPASS FILTER BASED ON EMULATION OF MAGNETICALLY-COUPLED RESONATORS *

4.1. Motivation and Background

A lot of research in the area of integrated active LC filters in a low-cost CMOS technology has been motivated by the need of highly integrated wireless communication transceivers. The requirement of high frequency RF bandpass filters with narrow fractional bandwidths for pre-selection, image rejection, and channel selection, has so far rendered the superheterodyne receiver unsuitable for monolithic integration. Several attempts can be found in the literature [58-62] to eliminate the off-chip passive filters and obtain a fully integrated solution which will reduce power consumption, area, cost, and need of impedance matching.

4.1.1 On-chip Inductors

The area that is required by the on-chip spiral inductor becomes reasonable at RF frequencies. An on-chip inductor is always laid out as a spiral metal trace in one or more of the metal layers available in the used technology.

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* Part of this chapter is reprinted with permission from "A 2.7V, 1.8GHz, 4th Order Tunable LC Bandpass Filter Based on Emulation of Magnetically-Coupled Resonators," by Ahmed N. Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, July 2003. *IEEE J. Solid-State Circuits*, vol. 38, no. 7.

Unfortunately, the spiral on-chip inductors have a lot of non-idealities and parasitic effects. The first parasitic effect is the inductor series resistance associated with the sheet resistance of the metal traces used to layout the inductor. This resistance is even larger at high frequencies due to the skin effect. The second parasitic effect is the parasitic capacitance to the substrate causing the inductor to self-resonate at a certain frequency beyond which the inductor behaves as a capacitor. The third parasitic effect is the eddy currents causing losses in the underlying substrate. This effect is more prominent in heavily doped, i.e., low resistively substrates.

All of the previously mentioned loss mechanisms contribute to the degradation of the overall quality factor of on-chip inductors. A lot of work has been done to improve the performance of on-chip inductors by optimizing the technology or using special processing techniques [63].

Another alternative implementation that alleviates the problems of planar inductors is using the parasitic inductance of the package bonding wire. Bond wires exhibit higher Qs than their on-chip spiral counterparts. Nevertheless, their usage is constrained by the limited range of realizable inductance, large production fluctuations and large parasitic (bond pad) capacitance. On the other hand, spiral inductors exhibit good matching and are therefore attractive for commonly used differential architectures. Furthermore, they permit a large range of inductance to be realized.

Form the circuit design point of view, a physical model for on-chip inductors is needed. This is not an easy task, the difficulty of physical modeling stems form the complexity of high frequency phenomenon such as the eddy current effects. Each

element of the model should be representing a physical phenomenon occurring in the part of the structure it represents as the model shown in Fig. 4.1. The series inductor L_S and the series resistor R_S represent the inductance and resistance of the spiral, respectively. The direct capacitive coupling between the two terminals of the inductor is modeled by the series capacitance C_S. C_{OX} models the oxide capacitance between the spiral and the silicon substrate. The capacitance and resistance of the silicon substrate are modeled by C_{Si} and R_{Si}.

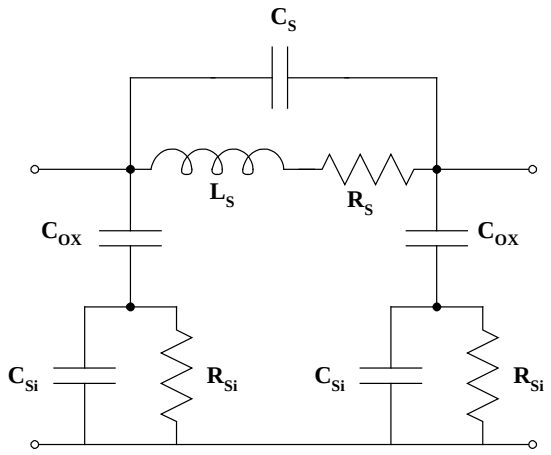


Fig. 4.1 A lumped circuit model of a spiral inductor on silicon

A lot of CAD electromagnetic simulators, such as ASITIC [69], that are capable of representing the electromagnetic fields have been developed to provide the circuit designer with the required physical mode. The simulator input is a number of parameters that characterize the inductor. These include the number of turns, the width of metal tracks, the spacing between tracks, the length of the first outer segments, the number of metal layers and finally the type of structure (number of metal layers, in series, in

parallel, octagonal, etc.). After the geometry of the spiral inductor is defined, the necessary parameters of the technology process are provided, and the simulator generates a circuit model that can be directly used in spice simulation. The simulator also provides information about the value of the inductance and the quality factor of the given inductor's geometry. It is usually a trial and error procedure of simulating a pool of inductors and choosing the inductor with the highest quality factor [70].

4.1.2 High Order Filters

To provide acceptable image rejection when the filtered signal is down converted to IF, high-order filters should be used. Classic LC filter synthesis can be used with Q-enhancement (discussed in section 4.2) applied to compensate for the LC tank losses [58-60]. This does not guarantee that the filter frequency response will be preserved.

In order to obtain a higher order filter and to avoid large element value spread, especially for the case of narrow band filters, coupled resonators are usually used [20,32,60]. A coupled filter consists of reactive parallel tank circuits, which are coupled together by capacitors, inductors, or magnetically as shown in Fig. 4.2 [64].

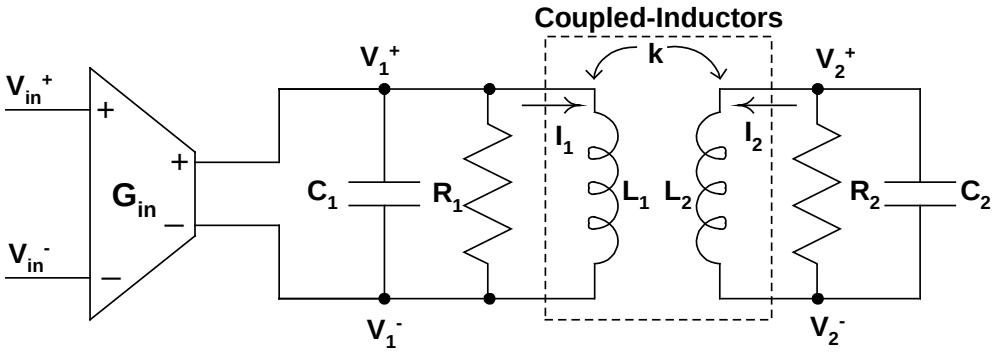


Fig. 4.2 Two magnetically-coupled resonators

For the case of magnetic coupling, the center frequency remains nearly fixed even if the coupling coefficient k is changed. For fixed termination resistors insertion loss becomes lower with increasing the coupling coefficient towards the critical coupling. In the proximity of critical coupling, the bandwidth becomes larger with a flat passband response and finally, with a further increase in the value of coupling, passband ripple will appear as shown in Fig. 4.3.

The filter's center frequency ω_0 is determined by the resonance frequency of the resonators. The magnetic coupling coefficient k determines the filter's bandwidth BW. In order to avoid insertion loss and passband ripple, the termination resistance is chosen to achieve the case of critical coupling (flat passband response) [64]. Assuming identical resonators, the filter design equations are:

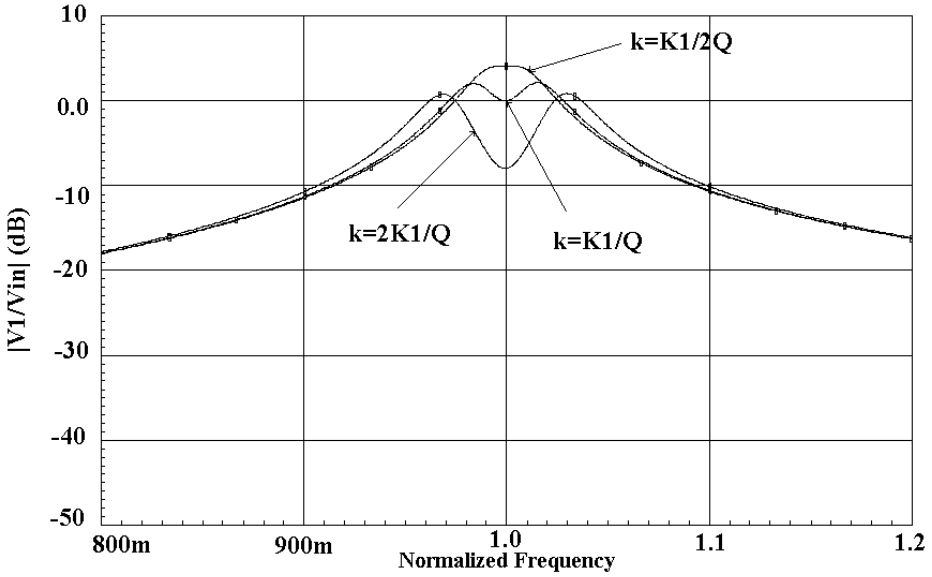
$$LC = (1/\omega_0^2) \tag{4.1}$$

$$k = K_1(BW/\omega_0) = K_1/Q \tag{4.2}$$

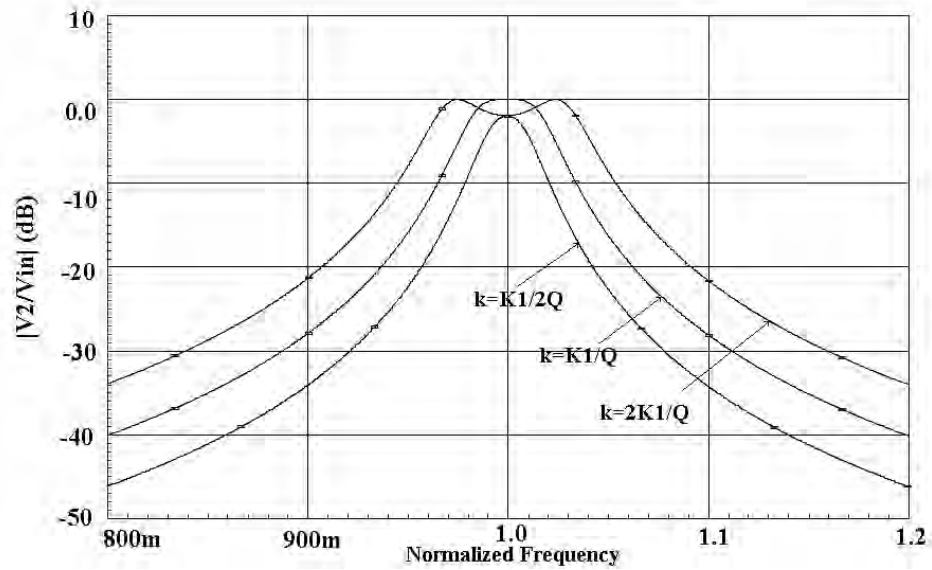
$$R = R_1 = R_2 = K_2 Q\sqrt{L/C} \tag{4.3}$$

where Q is the required filter quality factor[1]; K_1 and K_2 are constant values that depend on the filter approximation used and the number of resonators. For a Butterworth approximation with two resonators, K_1 and K_2 can be found from tables [64] to be $(1/\sqrt{2})$ and $\sqrt{2}$ respectively.

[1] Q is defined as the ratio of the center frequency to the –3dB bandwidth of the filter



(a)



(b)

Fig. 4.3 Ideal transfer functions (a) $|V_1/V_{in}|$ (dB) (b) $|V_2/V_{in}|$ (dB)
f_0=1, BW=0.04 (Q=25), and k={K_1/2Q, K_1/Q, 2K_1/Q}
Case of critical coupling k=K_1/Q

Fig. 4.4 shows the effect of changing the termination resistance R while fixing Q=25, or equivalently fixing k. For the value of R given by equation (4.3), the output magnitude response is flat in the passband. Changing the value of R has almost no effect on the bandwidth but the flatness of the passband and peak gain are greatly affected.

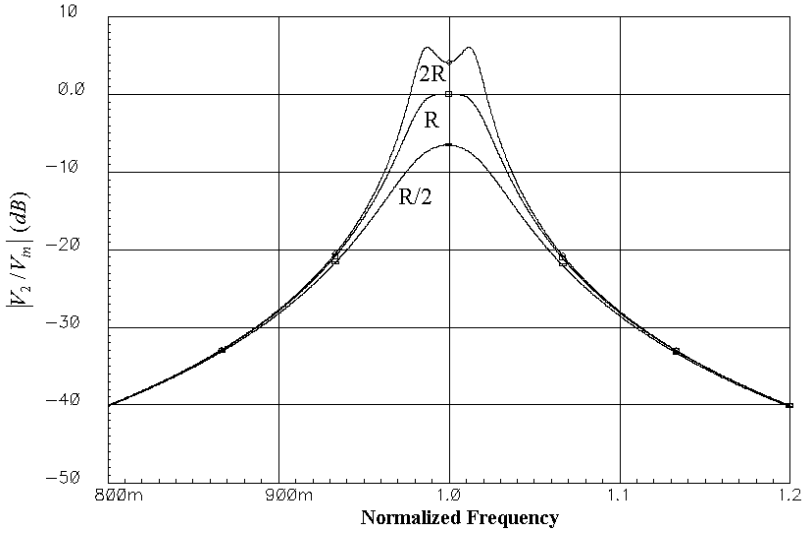


Fig. 4.4 Tuning termination resistance {R/2,R,2R} (fixed Q=25)

Thus to maintain the passband flatness while tuning the bandwidth (changing the value of k), according to equations (4.2) and (4.3), both k and R needs to be tuned simultaneously such that the product kR is kept constant, as shown in Fig. 4.5.

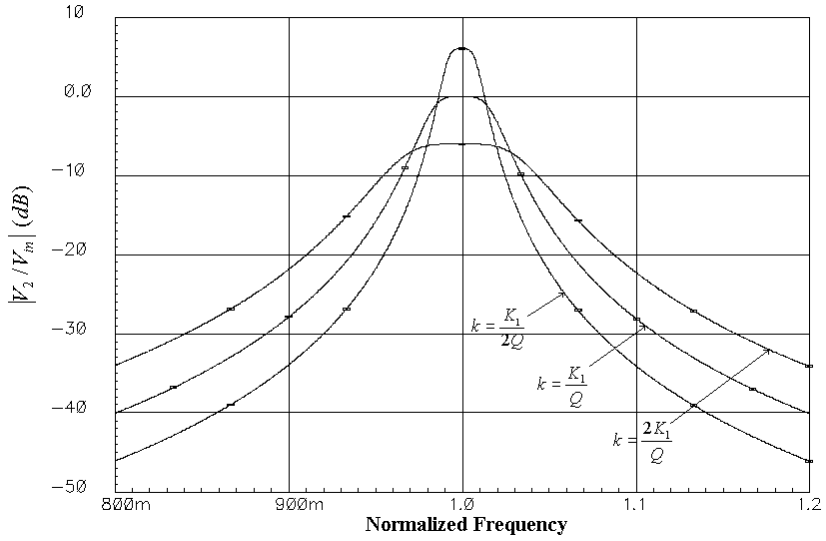


Fig. 4.5 Tuning k and R simultaneously (fixed k×R) k={K_1/2Q, K_1/Q, 2K_1/Q}

In this chapter, a new 4th order bandpass filter architecture is proposed [67-68] to avoid the drawbacks of the previously reported similar structures while also providing bandwidth tunability. The Q-enhancement approach is reviewed in section 4.2. Section 4.3 shows the evolution of the filter architecture from the two magnetically coupled resonator prototype. Section 4.4 discusses different trade-offs and design considerations of linearity and noise performance of the filter. The strategies for frequency and bandwidth tuning of the filter are presented in section 4.5. The experimental results are given in section 4.6. Finally, concluding remarks are drawn in section 4.7.

4.2. Q-enhancement Approach

As discussed earlier, due to the losses associated with integrated spiral inductors implemented in standard CMOS technologies, the achievable quality factor in the RF

range is limited. Hence to implement on-chip narrow band LC filters, positive feedback is needed to compensate for the losses, thus enhancing the Q of the filter; this is equivalent to adding a negative resistance. The negative resistance can be connected in parallel [58] or in series [59] with the inductor. For the former case, as shown in Fig. 4.6, the overall transfer function is given by:

$$\frac{V_0}{V_{in}}(s) = G_{in}\frac{R_L + sL}{(1 - G_m R_L) + s(CR_L - G_m L) + s^2 LC} \tag{4.4}$$

The center frequency ω_0 and the quality factor Q of the second order filter are given by:

$$\omega_0 \cong \frac{1}{\sqrt{LC}}\sqrt{1 - G_m R_L} \tag{4.5}$$

$$Q \cong \frac{Q_{ind}}{1 - (G_m / G_{loss})}\sqrt{1 - \frac{1}{Q_{ind}^2}} \tag{4.6a}$$

where

$$Q_{ind} = \frac{1}{R_L}\sqrt{\frac{L}{C}} \tag{4.6b}$$

and

$$G_{loss} \cong \frac{1}{Q_{ind}^2 R_L} \cong R_L(\omega_o C)^2 \tag{4.7}$$

For the case of narrow band filters, i.e., $Q >> Q_{ind}$, we have $G_m \cong G_{loss}$, and equation (4.5) can be written as:

$$\omega_0 \cong \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{1}{Q_{ind}^2}} \tag{4.8}$$

Note that due to the losses of the inductor there is a deviation in the frequency response of the filter even after using Q-enhancement. There is a shift in the filter center frequency and in the filter quality factor from their nominal values.

A typical value Q_{ind} (the quality factor of the on-chip inductors) of 4 results in a deviation of 3% of ω_0. This type of deviation in frequency response can be corrected by the automatic tuning circuit used to compensate normal IC component tolerances and temperature variations.

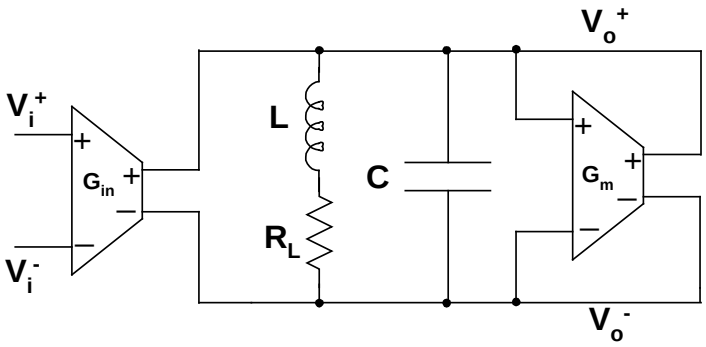


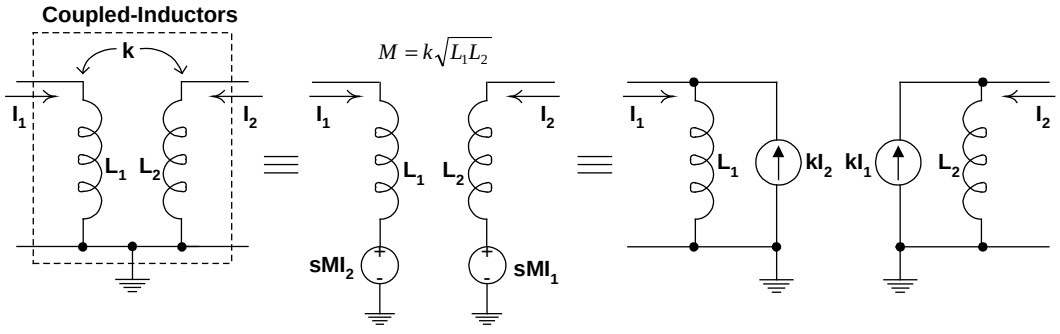
Fig. 4.6 Q-enhanced LC resonator

4.3. Filter Architecture

The filter structure is based on the emulation of two magnetically coupled resonators (double-tuned transformer prototype) shown in Fig. 4.2. In contrast to the previously published works [20,32,60], the proposed filter has a very small bandpass ripple (less than 0.5 dB). It also provides the possibility of tuning the filter bandwidth without affecting much the flatness in the passband. This is achieved by emulating the action of the coupled-resonators using a current sensing element (a resistor) and a tunable coupling transconductance.

4.3.1 Effects of Non-Ideal Inductors

For ideal coupled-inductors, magnetic coupling results in an induced current in one resonator, which is in phase with the current in the opposite inductor, as shown in Fig. 4.7. However, with non-ideal on-chip inductors, the inductor currents and voltages are not in quadrature (even using Q-enhancement) due to the resonator losses, i.e., the induced current has in-phase and quadrature-phase components. This leads to severe passband asymmetries. To maintain a flatband response, the approach adopted in [32] was to incorporate a coupling neutralization circuit that injects current into one resonator proportional to the voltage in the opposite resonator to cancel the effects of the undesired coupling component. This approach needs at least one-time trim to get a passband ripple better than ±1dB. It also lacks the possibility of changing the magnetic coupling coefficient, which is a function primarily of inductor placement on the die. Thus the filter's bandwidth cannot be tuned, while keeping the flat passband response, to account for any process or temperature variations or to adapt to different wireless standards.



(a) (b) (c)

Fig. 4.7 Coupled-inductors models (a) Ideal, (b) Equivalent circuit based on CCVS (c) Equivalent circuit based on CCCS

The proposed approach adopted here is to emulate the action of the magnetic coupling. This can be done using current controlled voltage sources (CCVS) as shown in Fig. 4.7(b) or current controlled current sources (CCCS) as shown in Fig. 4.7(c). In the first realization, the current should be sampled in one inductor and a quadrature-phase voltage is applied to the opposite inductor. This realization has two drawbacks. First, a 90^0 phase shift needs to be implemented and second, the output resistance of the CCVS should be very small compared to the losses of the inductor. In order to simplify the implementation, the second realization is adopted. The proposed CCCS has been implemented by sensing the current in one inductor, using a small resistor R_S, and injecting an in-phase current to the opposite resonator using the tunable transconductance G_k, i.e., $k=R_S G_k$.

Thus the proposed 4^{th} order filter, using electric coupling to emulate the coupled-inductors, based on the prototype of Fig. 4.2 becomes Fig. 4.8 for $k<<1$. R_L is the series resistance associated with the losses of the inductor. This is done placing the inductors apart from each other such that the physical magnetic coupling is diminished. It has been verified using the magnetic simulator ASITIC that if the inductors are placed at a distance four times that of their diameter, the coupling coefficient k is less than 0.1%. The proposed approach not only eliminates the need of any extra neutralization circuit but it also gives the flexibility of tuning the bandwidth without affecting the flatness in the filter's passband.

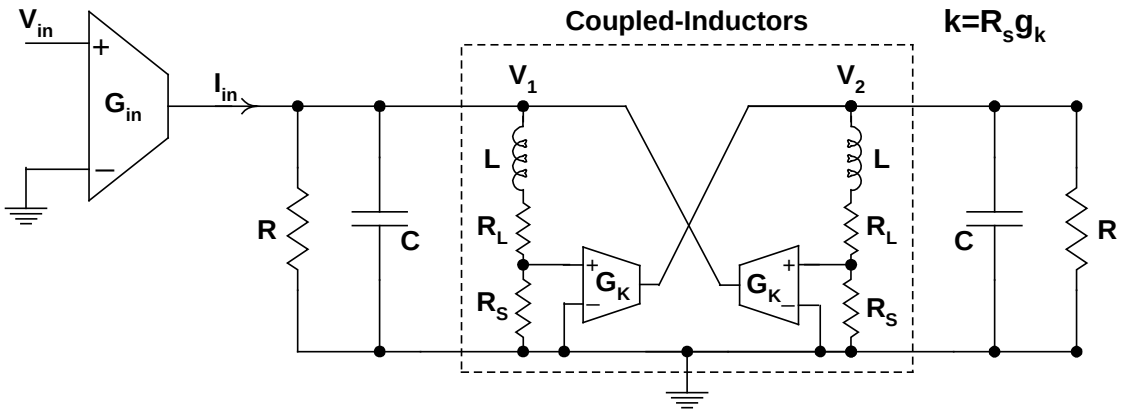


Fig. 4.8 Proposed 4th order filter with electric coupling to emulate the coupled-inductors

4.3.2 Effect of Mismatches

In this section, the effects of mismatches between the two resonators on the filter response (especially passband ripple) are investigated. Fig. 4.9 and Fig. 4.10 show the frequency response of the first resonator, the second resonator, and the total filter for different mismatch values between the two resonators. The mismatch is introduced in the value of the capacitor in one of the resonators. It has been observed that introducing a mismatch in the value of the inductor has almost the same effect on the filter frequency response. Introducing x% mismatch in both the inductor and the capacitor has almost the same effect as introducing 2x% mismatch in either one of them. Note also that the center frequency of the two resonators is now different from the center frequency of the filter. Although the frequency response of the second biquadratic section is still symmetric but the frequency response of the first biquadratic section is unsymmetric, it has more peaking in one direction than in the other. Nevertheless the symmetry of the total frequency response is reserved for this kind of mismatch in the L or C.

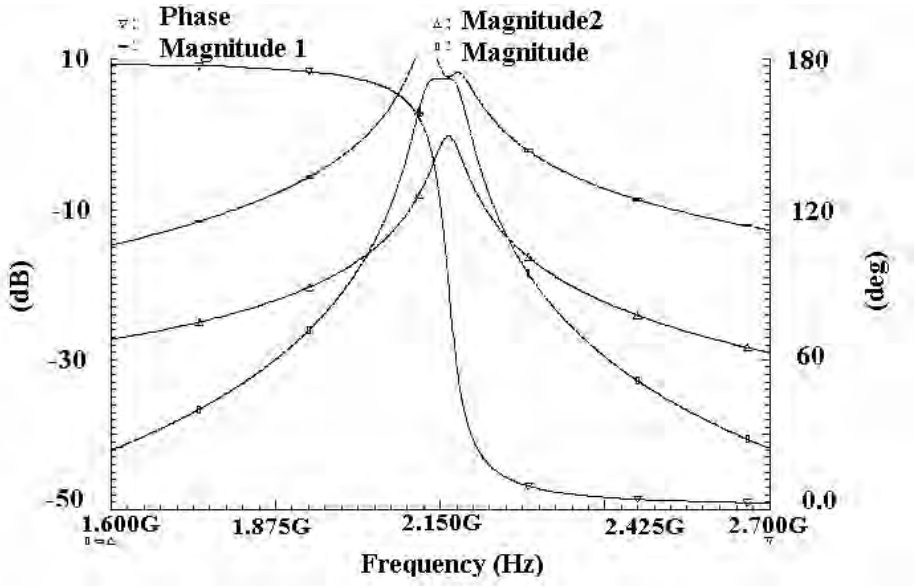


Fig. 4.9 Frequency response for 2% mismatch in LC

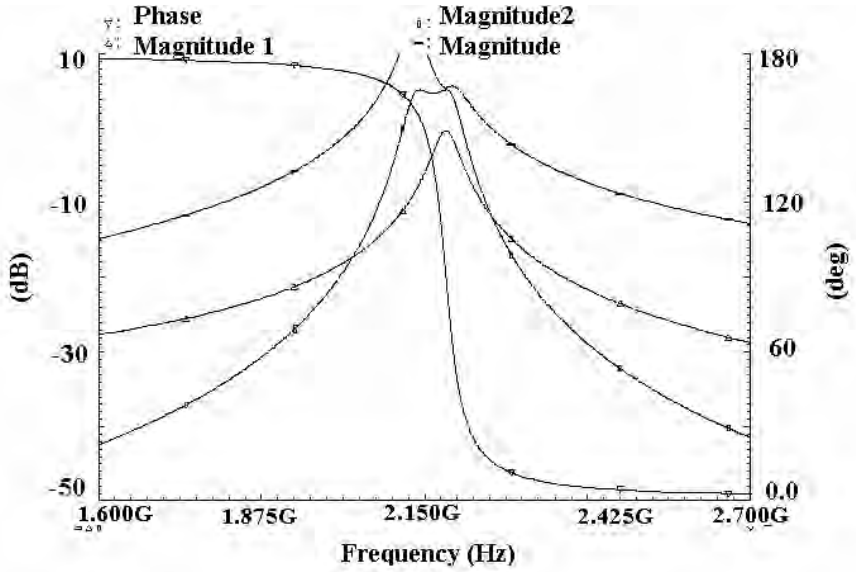


Fig. 4.10 Frequency response for 5% mismatch in LC

Table 4.1 shows the previous effect of mismatch on the passband ripple, passband gain, and percentage error in the center frequency.

Table 4.1 Effect of mismatch in the inductor or the capacitor

Mismatch	Passband Gain	Passband Ripple	% Error in f_0
0 %	8.5 dB	0 dB	0 %
2 %	7.4 dB	0.05 dB	1.1 %
4 %	4.7 dB	0.5 dB	2.1 %
6 %	1.4 dB	1.5 dB	3.3 %
8 %	-1.9 dB	2.7 dB	4.3 %
10 %	-5.0 dB	4.0 dB	5.6 %

Up to about 2% of mismatch, or equivalently 1% mismatch in both the inductor and the capacitor, the passband ripple is almost negligible (<0.1dB). The error in the center frequency is about 1%. Note that up to 4% of mismatch can be tolerated without too much degradation in the total frequency response. The passband ripple is less than 0.5dB and error in the center frequency is about 2%. A relationship between the tuning error ε, defined as the shift in the center frequency, and the mismatch can be also interpolated from the results of Table 4.1 as follows:

$$\varepsilon \cong \frac{\Delta L + \Delta C}{2} \tag{4.9}$$

where ΔL and ΔC is the percentage mismatch in the inductor and the capacitor respectively.

Another type of mismatch is investigated, the mismatch in the series loss resistor of the inductor, or equivalently the parallel negative resistance that is used for Q-enhancement. Fig. 4.11 and Fig. 4.12 show the frequency response of the first resonator,

the second resonator, and the total filter for different mismatch values between the two series resistors representing the losses in the inductors of the two resonators. Note that, on the contrary to the previous case, the mismatch in the loss resistor introduces some non-symmetry of the total frequency response, especially for high values of mismatches.

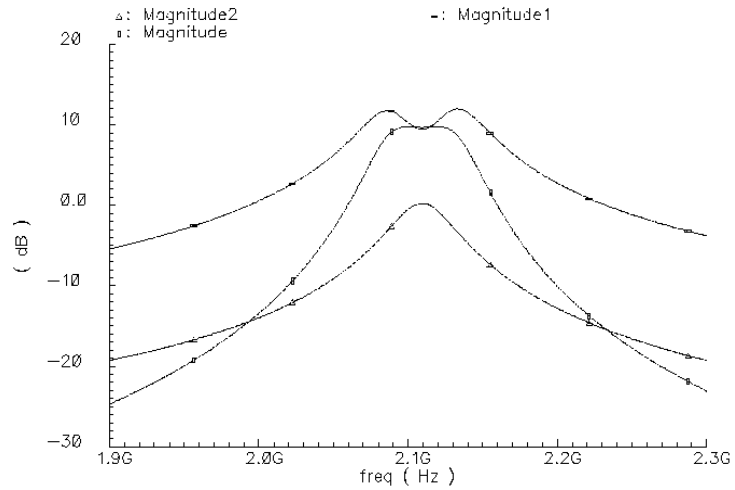


Fig. 4.11 Frequency response for 2% mismatch in R

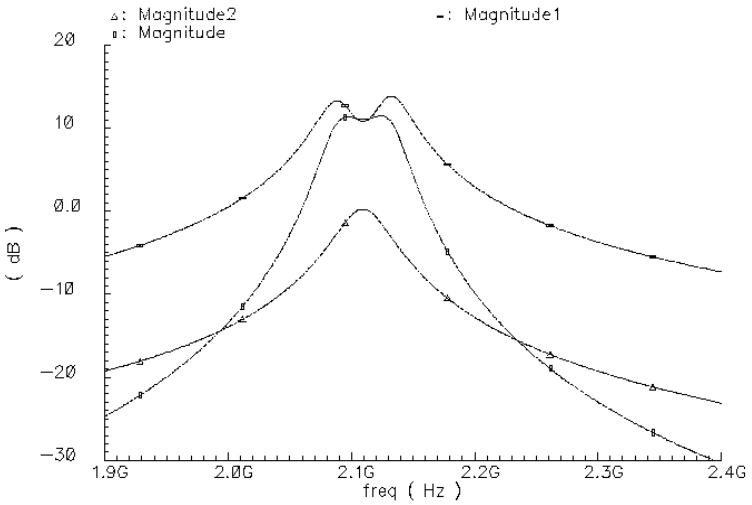


Fig. 4.12 Frequency response for 5% mismatch in R

Table 4.2 shows the previous effect of mismatch on the passband ripple, passband gain, and percentage error in the center frequency. The error in the center frequency depends on the square of the quality factor of the inductor. The error in the center frequency is almost constant at –1.6%. Note that up to 5% of mismatch can be tolerated without too much degradation in the total frequency response. The passband ripple is less than 0.5dB.

Table 4.2 Effect of mismatch in the series resistor

Mismatch	Passband Gain	Passband Ripple	% Error in f_0
0 %	8.5 dB	0 dB	0 %
2 %	9.7 dB	0.06 dB	-1.6 %
5 %	11.0 dB	0.33 dB	-1.6 %
8 %	12.7 dB	1.0 dB	-1.6 %
10 %	14.1 dB	1.8 dB	-1.6 %

Fig. 4.13 shows the frequency response for an introduced mismatch of 2% in the elements of one resonator with respect to the other (in the inductor, capacitor, and the loss resistor). The ripple in the passband is about 1dB. In conclusion, a mismatch of 2% in L and C can be tolerated. A mismatch in the value of the loss resistor does affect the symmetry of the magnitude response and create some ripples in the passband. A mismatch of 5% in the value of R can be tolerated. The mismatch errors cannot be corrected by the tuning scheme.

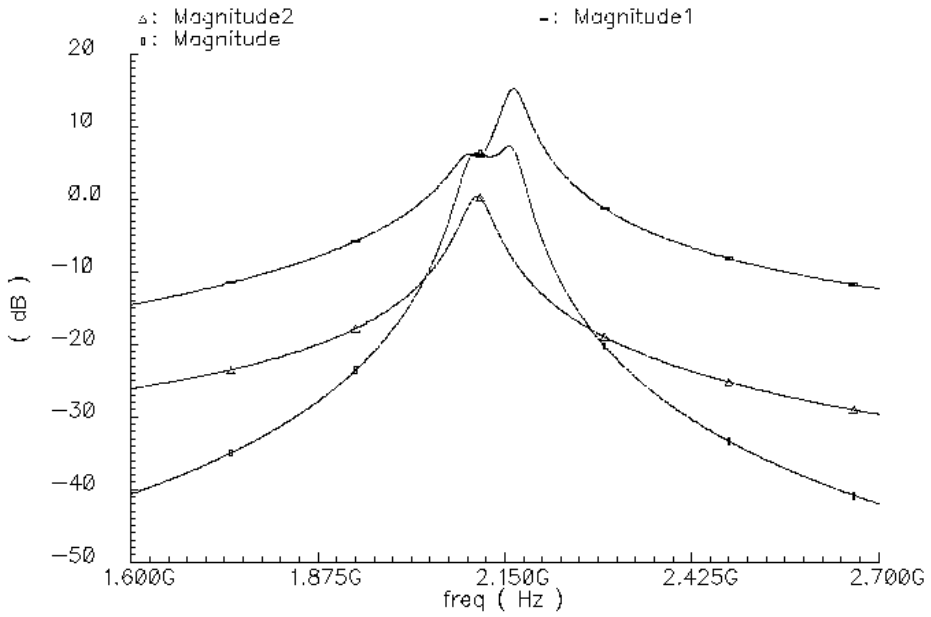


Fig. 4.13 Magnitude response for 2% mismatch in elements of one resonator

4.3.3 Design Equations

In Fig. 4.8, assuming that the two resonators are identical, it can be shown that:

$$\frac{V_2}{V_1} = -k\frac{1}{(1+GR_T)+s(GL+R_TC)+s^2LC} \tag{4.10}$$

where $R_T=R_S+R_L$, and G=(1/R) represents the overall resistive termination.

In practical circuits G is the combination of the resistive termination and the negative transconductance ($-1/Q_0^2R_T$) used for Q-enhancement to compensate for the inductor losses (including R_S and R_L). Thus according to equations (4.8) and (4.10), we can write:

$$G = \frac{1}{K_2}\frac{1}{Q}\sqrt{\frac{C}{L}} - \frac{1}{Q_0^2R_T} = \frac{1}{Q_0R_T}\left[\frac{1}{K_2Q} - \frac{1}{Q_0}\right] \tag{4.11}$$

where

$$Q_0 = \frac{1}{R_T}\sqrt{\frac{L}{C}} = \frac{1}{(R_S + R_L)}\sqrt{\frac{L}{C}}\text{, i.e, } Q_0 = \frac{R_L}{(R_L + R_S)}Q_{ind} \tag{4.12}$$

For $Q>(Q_0/K_2)$, G is a negative conductance. This condition is always satisfied for high Q filters. As described in equation (4.6), there is a shift in the filter's center frequency ω_0.

The transimpedance transfer functions, of Fig. 4.8, can be derived as follows:

$$Z_1(s) = \frac{V_1}{I_{in}}(s) = \frac{\left[1 + GR_T + s(GL + R_T C) + s^2 LC\right]\left[R_T + sL\right]}{\left[1 + GR_T + s(GL + R_T C) + s^2 LC\right]^2 - k^2} \tag{4.13}$$

$$Z_2(s) = \frac{V_2}{I_{in}}(s) = -k\frac{(R_T + sL)}{\left[1 + GR_T + s(GL + R_T C) + s^2 LC\right]^2 - k^2} \tag{4.14}$$

The passband voltage gain A_v at ω_0 is given by:

$$A_v = \left|\frac{V_2}{V_{in}}(j\omega_0)\right| = \left|\frac{V_1}{V_{in}}(j\omega_0)\right| \cong \frac{1}{\sqrt{2}}Q.G_{in}.\omega_0.L \tag{4.15}$$

4.3.4 Circuit Implementation

The proposed circuit implementation of the filter is shown in Fig. 4.14. Cross-coupled transistors M_1 compose the negative transconductance G. The coupling transconductance G_k is composed of transistors M_2, and input transconductance is

composed of transistors M_{in}. R_S is the sensing resistance and is implemented as a polysilicon resistance. The inductors use the three available metal layers in series. Each inductor has 2.5 turns/layer with an inductance value of 3nH, an equivalent series resistance (including Eddy current losses in the substrate) of R_L=12.5Ω, and occupies an area of 85μm×85μm. The varactor used is an accumulation mode PMOS capacitor. Connecting the drain and source to the lowest DC voltage ensures that the formation of inversion region is inhibited.

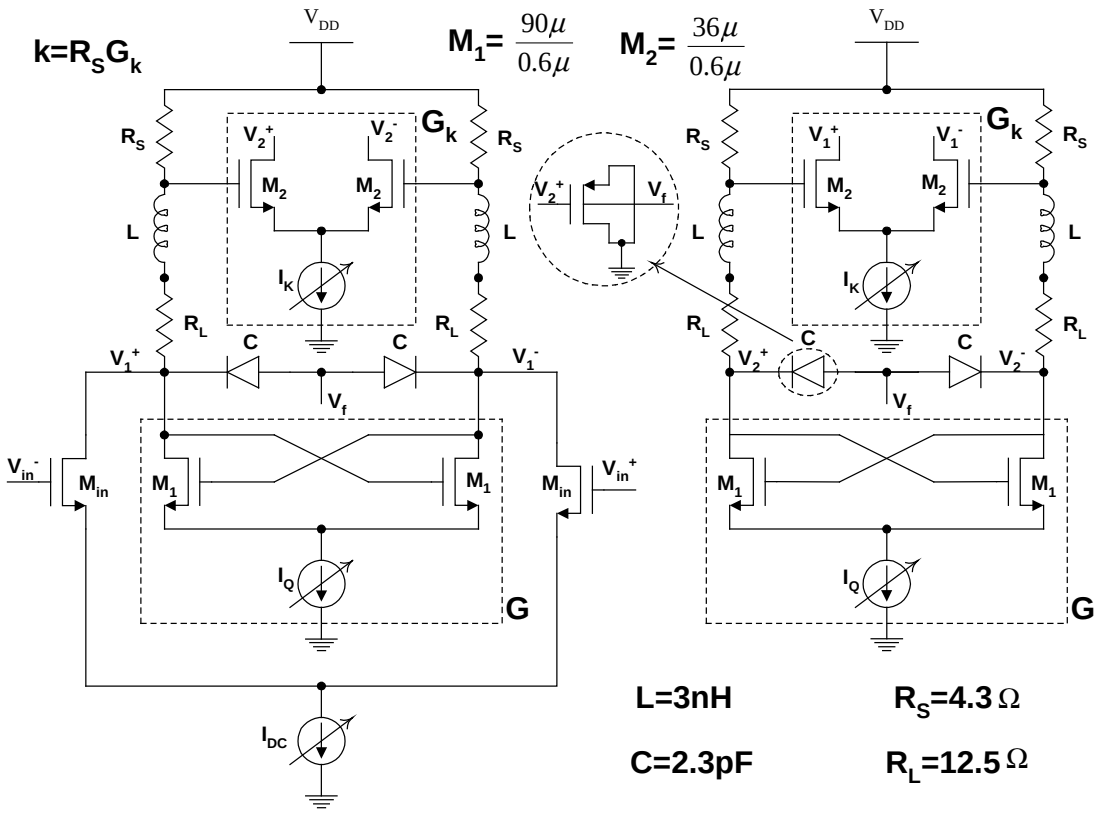


Fig. 4.14 Proposed filter circuit implementation

4.4. Design Considerations

In this section different design trade-offs to optimize the filter's power consumption and dynamic range are discussed.

4.4.1 Power Consumption

Fig. 4.15 shows the factor $G_{tot}^2 R_L^2=(G_k^2+G^2) R_L^2$, which is proportional to the power consumption, as a function of the ratio R_S/R_L, for $Q_{ind}=2.7$ and $Q=25$. Note that increasing the value of R_S requires a larger value of G for the same R_L, and reducing the value of R_S requires a larger value of G_k for the same k. Thus the value of R_S should be carefully chosen. It can be shown that the value of R_S which minimizes $(G_k^2+G^2)\cong\left(\frac{1}{Q^2R_S^2}+\frac{1}{Q_{ind}^4(R_L+R_S)^2}\right)$ for a fixed R_L is given by:

$$R_S \cong R_L\left(\frac{Q_{ind}^4}{2Q^2}\right)^{1/3} \tag{4.16}$$

where Q_{ind} was defined in equation (4.6b).

As predicted by equation (4.16), for this application, the minimum occurs at $R_S/R_L\cong 0.35$. At the optimum value of R_S, the power consumption is dictated by the negative transconductance G. Also from Fig. 4.15, it can be seen that the required value of G_{tot}^2 is almost double that of the case where $R_S=0$ (magnetically coupled resonators), i.e, $G_{tot}^2 = 2G^2\big|_{R_S=0}$. This can be realized by doubling the width of the transistors M_1 at the expense of reducing the tuning range, or by doubling the current I_Q at the expense of increasing the power consumption. A better trade-off is partially increasing both, which

will also keep a constant saturation voltage (constant linearity performace of the negative transconductance G); increasing the dimensions of M_1 by 40% and the current I_Q by 40%. It can be demonstrated that for higher Q, the percentage of power consumption increase, relative to the conventional case of magnetic coupling (R_S=0) is less. For example, at Q_{ind}=2.7 and Q=100, $G_{tot}^2 = 1.3G^2\big|_{R_S=0}$. This represents 15% increase in both the dimensions of M_1 and the current I_Q.

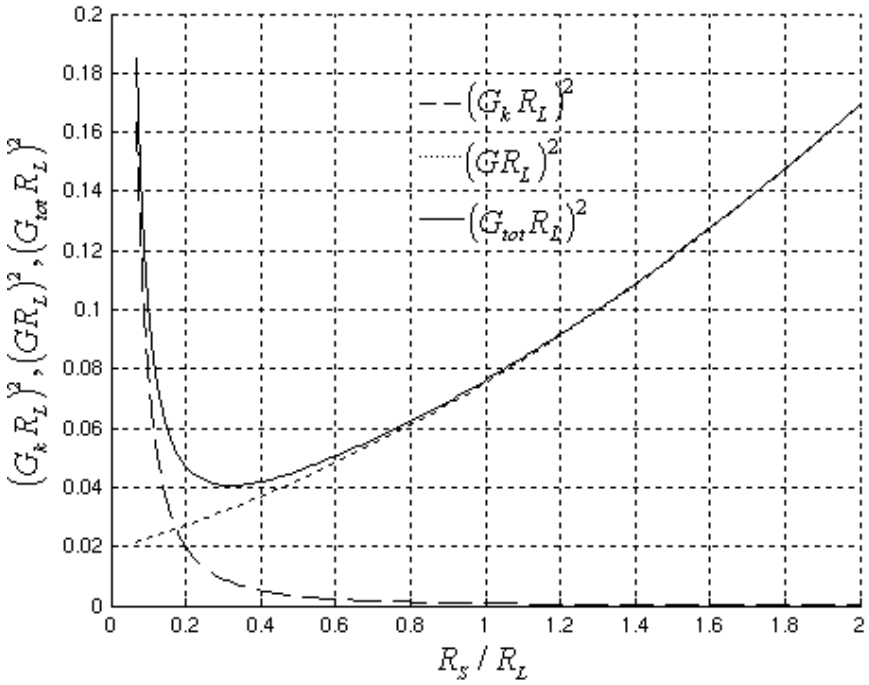


Fig. 4.15 Effect of R_S on the overall filter power consumption

4.4.2 Noise Analysis

The total integrated input referred mean square noise voltage, of the filter structure shown in Fig. 4.14, is calculated as follows:

$$v_{noise}^2 = \frac{1}{A_v^2}\left[\begin{array}{r} \frac{8}{3}KTG_{in}\int_0^\infty |Z_1(f)|^2 df + 4KTG_{loss}\int_0^\infty |Z_1(f)|^2 df + \frac{8}{3}KT|G|\int_0^\infty |Z_1(f)|^2 df \\ + \frac{8}{3}KTG_k\int_0^\infty |Z_1(f)|^2 df + 4KTG_{loss}\int_0^\infty |Z_2(f)|^2 df \\ + \frac{8}{3}KT|G|\int_0^\infty |Z_2(f)|^2 df + \frac{8}{3}KTG_k\int_0^\infty |Z_2(f)|^2 df \end{array}\right] \quad (4.17)$$

where $Z_1(f) = \frac{V_1}{I_{in}}(f)$, $Z_2(f) = \frac{V_2}{I_{in}}(f)$, and A_v^2 are given in equations (4.13), (4.14), and (4.15) respectively, factor γ accounts for the excess noise of short-channel devices.

The noise contributions shown in equation (4.17) are of the input transconductance G_{in}, the inductor loss G_{loss}, the negative transconductance G, and the coupling transconductance G_k, respectively. It can be shown that:

$$\int_0^\infty |Z_1(f)|^2 df \cong 2.|Z_1(f_0)|^2 . \frac{\pi}{2}\frac{f_0}{Q} = \frac{Q^2}{(\omega_0 C)^2} \times BW_{eff} = \frac{1}{4}\frac{Q}{\omega_0 C^2} \quad (4.18)$$

Also, let us define:

$$\alpha = \frac{\int_0^\infty |Z_2(f)|^2 df}{\int_0^\infty |Z_1(f)|^2 df} \quad (4.19)$$

where α (<1) is a factor that accounts for the noise shaping of the noise contributions of the first resonator by the transfer function given in equation (4.10). For this design α is about 0.3. Substituting equations (4.18) and (4.19) in (4.17), and for $G \cong -G_{loss}$, i.e., the case of narrow band filters, we obtain:

$$v_{noise}^2 \cong \frac{8\gamma}{3} KT \times BW_{eff} (1+\alpha)\left[\frac{1}{(1+\alpha)G_{in}} + 2.5\frac{G_{loss}}{G_{in}^2} + \frac{G_k}{G_{in}^2}\right]$$
$$\cong \frac{(1+\alpha)\gamma}{A_v^2}\frac{2KT}{3C}\frac{Q}{Q_0}\left[\frac{1}{(1+\alpha)}\frac{G_{in}}{G_{loss}} + 2.5 + \frac{G_k}{G_{loss}}\right] \quad (4.20)$$

where K is boltzman's constant, T is temperature in degree kelvins.

Note that there is a trade-off in choosing the value of R_S for noise performance. Increasing the value of R_S implies reducing Q_0, see equation (4.12), and consequently increasing the noise contribution of G_{loss} and G. Reducing the value of R_S implies increasing the value of G_k (for the same k) and consequently increasing its noise contribution. Thus R_S must be judiciously chosen as a trade-off to minimize the total integrated input referred noise. For the case of low peak gain, i.e., $A_v<(K_1Q/Q_0)$, or equivalently $G_{in}<G_{loss}$, the noise contribution of the input transconductance, $1/[(1+\alpha)G_{in}]$ in equation (4.20), can be neglected. Thus according to equation (4.20), R_S should be chosen to minimize $G_T=(2.5G_{loss}+G_k)$. This leads to the following condition, for the case of $A_v<(K_1Q/Q_0)$, to minimize the total integrated input referred noise power for a fixed

$$R_S \cong R_L\left(\frac{Q_{ind}^2}{2.5\sqrt{2Q}}\right)^{1/2} \quad (4.21)$$

Fig. 4.16 shows the factor G_TR_L(solid line), which is proportional to the integrated noise power, as a function of the ratio R_S/R_L, for $Q_{ind}=2.7$ and Q=25. As predicted by equation (4.21) the minimum occurs at $R_S/R_L\cong0.28$. Note that at the optimum value of R_S, the power consumption is dictated by the negative transconductance G and the inductor losses G_{loss}. Around the optimum value of R_S, the inductor loss and the negative transconductance dominate the noise performance. Note also that there is about 25%

increase in the integrated noise voltage than the case where R_S=0, i.e., magnetically coupled resonators. This is equivalent to a 1.76dB deterioration in the noise figure of the filter. As the case for power optimization, it can be demonstrated that for higher Q, the percentage increase in the integrated noise voltage, relative to the conventional case of magnetic coupling (R_S=0), is less. For example, the integrated noise voltage increases by 12% only for the case of Q_{ind}=2.7 and Q=100. The inverse is true for Q_{ind}, i.e., for higher Q_{ind} the percentage increase in the integrated noise voltage, relative to the conventional case of magnetic coupling is more. This can be explained since as Q_{ind} goes to infinity, G goes to zero but G_k does not.

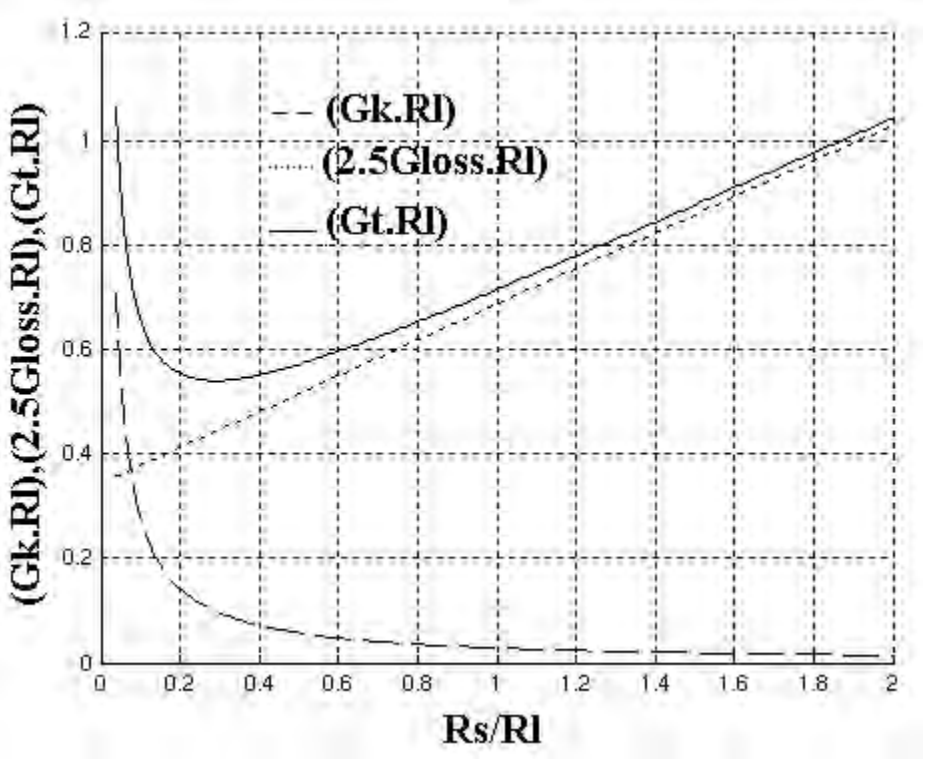


Fig. 4.16 Effect of R_S on the overall filter noise performance

Since the integrated noise power is fairly constant for values of R_S/R_L from 0.2 to 0.3, the value of R_S can be chosen to minimize the power consumption. This results in R_S of 4.3Ω, and a coupling transconductance in the order of 6.5mS for Q=25.

Note that as the quality factor Q_{ind} of the inductor increases, a lower negative transconductance is required for a given filter Q, specified by the selectivity requirements of the system. This in turn decreases the noise contribution of the negative transconductance, in addition to the reduced noise contribution of the inductor itself. Another advantage of using an inductor with a high quality factor (small G_{loss}) is a reduction in the power consumption mainly dictated by the negative transconductance used to compensate for the losses assumed mainly of the inductor.

4.4.3 Nonlinearity Analysis

To isolate the effect of the nonlinearities in this analysis, each nonlinear element is considered separately [65], i.e., assuming all other elements are linear. It is also assumed the nonlinearities injected from one resonator to the other are negligible. This is a reasonable assumption due to the fact that small current sensing resistor R_S has a small voltage across it. Assuming that the input transconductance (G_{in}) is the only source of nonlinearity, the filter input 1dB compression point, for a long-channel approximation, is given by:

$$V_{1-dB,in}^2 = V_{1-dB}^2\Big|_{G_{in}}, \text{ where} \tag{4.22}$$

$$V_{1-dB}\Big|_{G_{in}} = 1.077\times(V_{GS}-V_T) = 1.077\times\sqrt{\frac{2I_{DC}}{K_n(W/L)_{in}}} \tag{4.23}$$

In equation (4.23) an input transconductance based on a coupled differential pair with tail current source I_{DC} is assumed. The filter input 1dB compression point, assuming that the negative transconductance is the only source of nonlinearity, can be expressed as [58]:

$$V_{1-dB,G}^2 = \frac{V_{1-dB}^2\Big|_G}{A_v^2} \cdot \frac{Q_0}{Q} \tag{4.24}$$

$V_{1\text{-}dB|G}$ is defined as in equation (4.23) with transistor dimensions of $(W/L)_1$ and tail current of I_Q.

Note that the nonlinearity contribution of the input (G_{in}) and coupling (G_k) transconductances can be neglected with respect to that of the negative transconductance. This is true because for high Q or high gain applications, the voltage swing across the negative transconductance is much greater than the voltage swing across the coupling and input transconductances. Thus the best investment to improve the linearity performance of the filter is to linearize the negative transconductance, for example using source degeneration at the expense of more power consumption.

Assuming that the varactor (implemented as a MOSFET gate capacitance C_g) is the only source of nonlinearity, analysis yields the following expression for the input 1dB compression point of the filter:

$$V_{1-dB,C_g}^2 \cong \frac{0.145}{A_v^2 Q} \frac{1}{\left[(a_2/a_0)^2 + 4Q^2(a_1/a_0)^4\right]^{1/2}} \tag{4.25}$$

where a_1, and a_2 are the first and the second order nonlinearity coefficients in the power series expansion of the varactor capacitance-voltage characteristic, i.e., $C_g=a_0+a_1V+a_2V^2$, around a bias voltage V_R, respectively. $a_0=C_g(V_R)$ is the quiescent

value of the varactor capacitance. The exact values for a_0, a_1, and a_2 depend on the region of operation of the MOS transistor [66]. For low voltage applications, where V_R is limited by the supply voltage, the nonlinearity coefficients are large and the varactor contribution to the nonlinearity of the filter cannot be neglected.

The quality factor Q_{ind} of the inductor has a considerable effect on linearity as well. For a fixed filter quality factor imposed by the selectivity specification of the application, the higher Q_{ind}, the lower the loss conductance G_{loss}, assumed to be dominated by the inductor and consequently the lower the required negative transconductance. Thus, for a fixed tail current I_{DC} the dimensions of the cross-coupled transistors can be designed to allow for higher effective bias (V_{GS}-V_T) for better linearity [62].

Note also that increasing the input transconductance G_{in} reduces the input referred noise but on the other hand it increases A_v which reduces the 1dB compression point consequently resulting in an almost constant dynamic range. Noise-linearity is the first trade-off observed. The inverse dependence of the linearity to both the filter gain and quality factor in equations (4.24) and (4.25) shows that there is a selectivity-linearity trade-off as well. Although the simplified analytical expressions provided above ignore the interaction between different nonlinear elements, they are still useful as design guidelines for the trade-offs involved.

4.4.4 Dynamic Range

Assuming that the negative transconductance dominates the filter nonlinearity performance, the 1dB compression dynamic range (DR) of the filter can be written as:

$$DR = \frac{V_{1-dB,G}^2}{v_{noise}^2} = \frac{1.74 \times (V_{GS} - V_T)^2}{(1+\alpha) \times \gamma \times KT \left[\frac{1}{(1+\alpha)} \frac{G_{in}}{G_{loss}} + 2.5 + \frac{G_k}{G_{loss}} \right]} C \left(\frac{Q_0}{Q} \right)^2 \qquad (4.26)$$

This result shows that there is a factor of Q_0^2 improvement in the dynamic range of Q-enhanced LC filters over their OTA-C counterparts [60]. This is a main motivation for using LC filters in those RF applications where large dynamic range is required. The bandwidth used to determine the noise floor, in the previously derived DR expression, is the filter noise bandwidth. For a filter targeted to be used in a receiver, the bandwidth is usually taken to be the signal IF bandwidth which is normally less than the RF bandwidth. This will result in better dynamic range performance.

Note from equation (4.26) that the DR can be improved by maximizing (CQ_0^2). This implies, according to equation (4.12), maximizing (L/R_T^2). Assuming L and R_T scale proportionally, the dynamic range can still be improved by minimizing the losses of the inductor as low as possible. This can be achieved by using a small inductance, since it will certainly have smaller resistance. But the power consumption, mainly dictated by the negative transconductance is proportional to $R_T(\omega_0 C)^2$, as shown in equation (4.7), for a high Q filter where $G \cong -G_{loss}$. Thus using a small inductance will require large capacitance, for the same center frequency, and hence more power consumption. The inductance value cannot be very large either; this will result in a small capacitance leaving small room for an extra tunable varactor, and a limited tuning range.

4.4.5 Design Procedure

A simple design strategy for the LC resonator to maximize the tank dynamic range for a given power budget and a fixed center frequency could be itemized as:

1. Calculate the ratio R_S/R_L according to equation (4.16).
2. Choose the minimum inductance value to meet the power budget constraint, using equation (4.7).
3. Use a large $(V_{GS}-V_T)$ for the negative transconductance.

4.5. Filter Tuning Remarks

A major issue with LC filters, and continuous time filters in general, is the need of a tuning scheme required to compensate for the drift of element values (capacitors, inductors, and transconductors) due to process and temperature variations that will consequently affect the filter accuracy. The automatic tuning of an LC filter in the GHz range is a challenge and is still an open problem for investigation. In this section, some observed properties of the proposed filter architecture, that represent the information needed in an automatic tuning scheme for both the center frequency and quality factor, are presented and verified through experimental results.

Note from equation (4.10) that at the center frequency, the two voltages V_1 and V_2 are 90^0 out of phase. This is true for any value of coupling coefficient k or transconductance G. This represents the information needed for frequency tuning. The frequency tuning loop should be able to detect the phase difference between V_1 and V_2 and enforce it to be 90^0 at steady state by tuning the varactors.

Substituting equations (4.8) and (4.11) in (4.10), yields:

$$\frac{V_2}{V_1}(j\omega_0) = j\frac{1}{\sqrt{1-(1/Q_0^2)}} \cong j \tag{4.27}$$

Note that equation (4.27) represents the main information needed for bandwidth tuning while maintaining the flatness in the passband, i.e., case of critical coupling. For that case and exactly at the center frequency ω_0 the the two voltages V_1 and V_2 have the same magnitude.

The technique for tuning the bandwidth would be changing the coupling transconductance G_k to fix the coupling coefficient k to the required value of Q according to equation (4.7). This can be achieved by a separate tuning loop, as shown in Fig. 4.17. The bandwidth tuning loop should, simultaneously, enforce the magnitude of voltages V_1 and V_2 to be equal at steady state by tuning the negative transconductance G. Note that the tuning loop cannot correct the errors that are caused by mismatches between the two resonators.

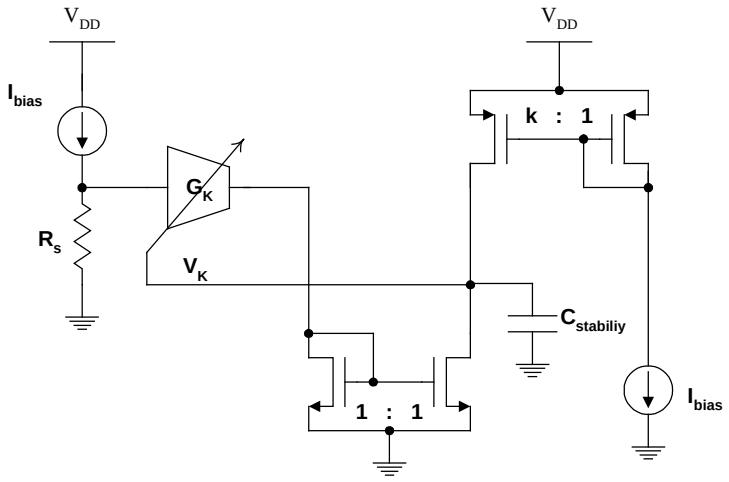


Fig. 4.17 Conceptual circuit for tuning the coupling coefficient k(=G_kR_S)

4.6. Measurement Results

A test chip filter has been fabricated in the HP 0.5μm CMOS process available through MOSIS. The chip micrograph is shown in Fig. 4.18. The filter and the additional on-chip buffers occupies an area of 500x300μm^2. Each inductor and each varactor occupies an area of 85x85μm^2 and 170x140μm^2, respectively. The inductors of opposite resonators are placed at 350μm apart to minimize their mutual coupling. The varactors are placed in the space between the resonators. All the shown measurements include the effect of the on-chip buffers with an estimated attenuation of 24dB (for 50Ω termination). The filter passband gain is tunable, through changing the current I_{DC}, with a programmability range of about 2:1, see Fig. 4.14.

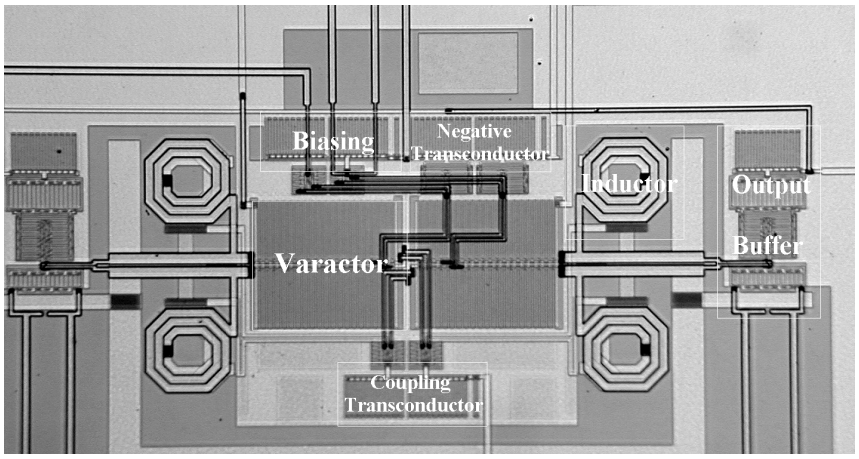


Fig. 4.18 Chip micrograph X=500μm, Y=300μm

When the bandwidth is tuned, by adjusting the current I_k, at 100MHz, the measured center frequency of the filter is tunable, by adjusting the voltage V_f, between 1.77-

1.86GHz as shown in Fig. 4.19. The measured filter's bandwidth is tunable between 70-100MHz, at a center frequency of 1.86GHz, as shown in Fig. 4.20.

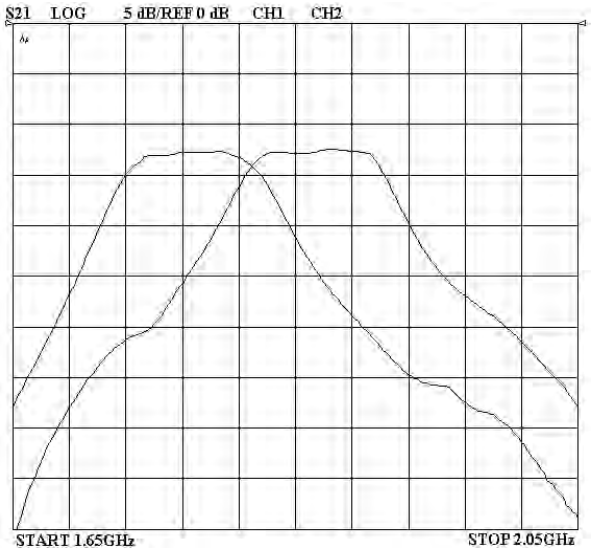


Fig. 4.19 Frequency tuning f_0={1.77GHz,1.86GHz}

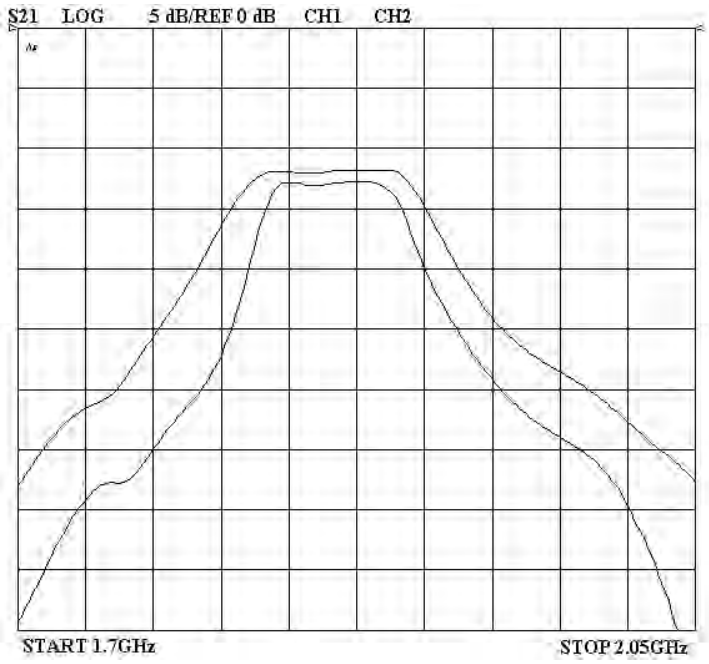


Fig. 4.20 Bandwidth tuning BW={70MHz,100MHz}

Fig. 4.21 shows the differential output of the two resonators with the center frequency and the bandwidth set at 1.846GHz and 80MHz respectively. Mismatches between the two resonators can be one of the reasons for asymmetry in the output of the first resonator (top trace). The filter's passband ripple is less than ±0.25dB. Note that the two outputs have equal magnitude at the center frequency. This result has been achieved by tuning manually the negative transconductance, by adjusting its tail current I_Q, to maintain the flatband response.

Fig. 4.22 shows the phase difference between the two filter outputs V_1 and V_2. Note that the two outputs are in phase quadrature (-90^0) at the filter's center frequency. The error in the center frequency is due to mismatches between the two resonators and is less than 0.05%.

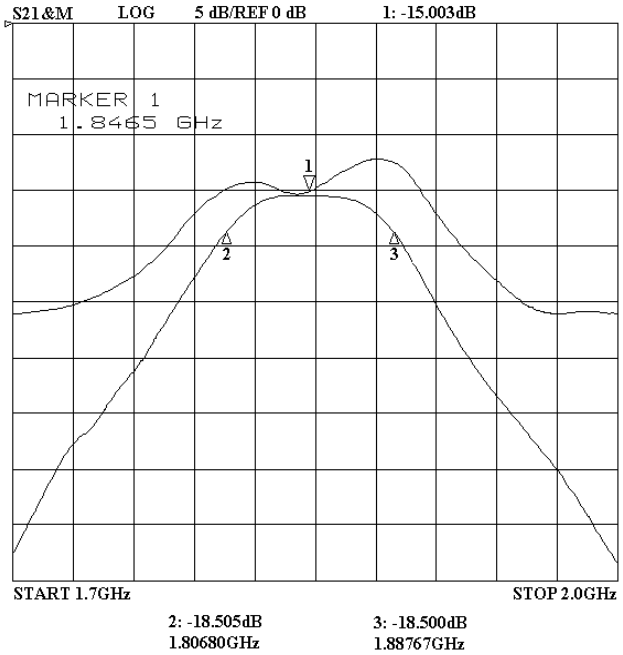


Fig. 4.21 Magnitude response, Upper trace $|V_1/V_{in}|$ (dB) Lower trace $|V_2/V_{in}|$ (dB)

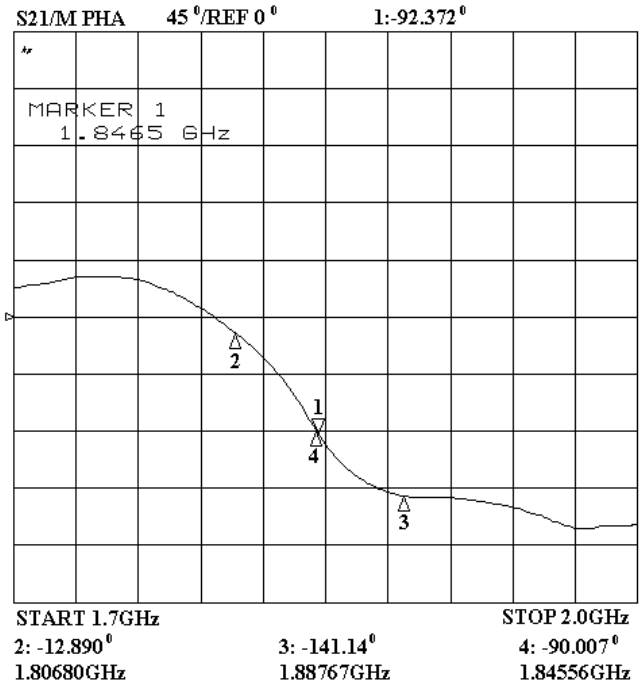


Fig. 4.22 Phase difference between the two filter ouputs V_1 and V_2

The two-tone intermodulation distortion measurement is shown in Fig. 4.23. The two tones are applied at 1.84GHz and 1.85GHz, and they have the same amplitude of -34dBm. The measured output 1dB compression point is -40dBm as shown in Fig. 4.24. As given by equation (4.24), the filter's input 1dB compression point can be calculated as -21dBm for V_{DSAT} of about 0.3V and Q_0/Q of about 0.1. The measured input 1dB compression point value, as shown in Fig. 4.24, is about -26dBm. The difference between the theoretical and measured values is expected since equation (4.24) does not take into account the nonlinearity contributions from the varactor, the input differential pair, the output buffer, and the interactions between the contributors.

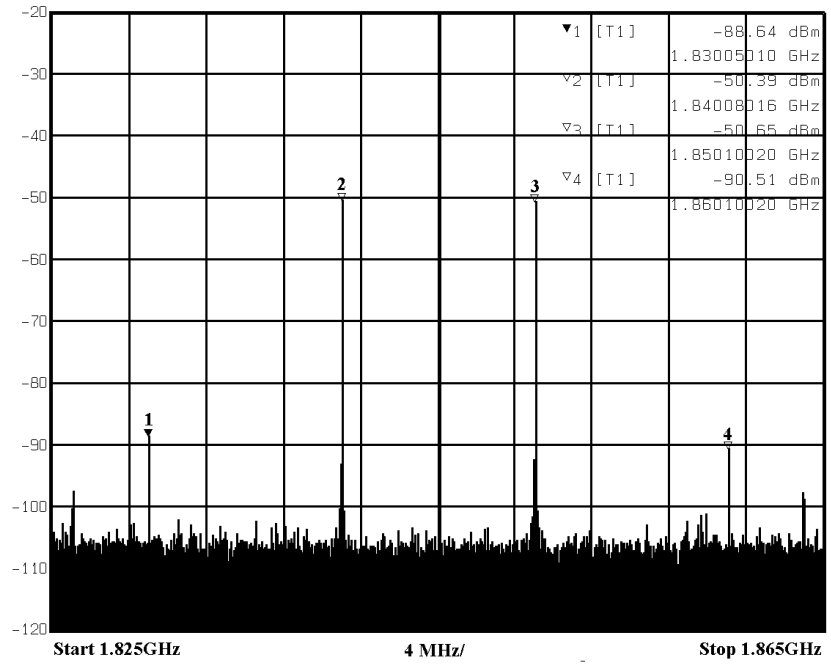


Fig. 4.23 Two-tone intermodulation distortion

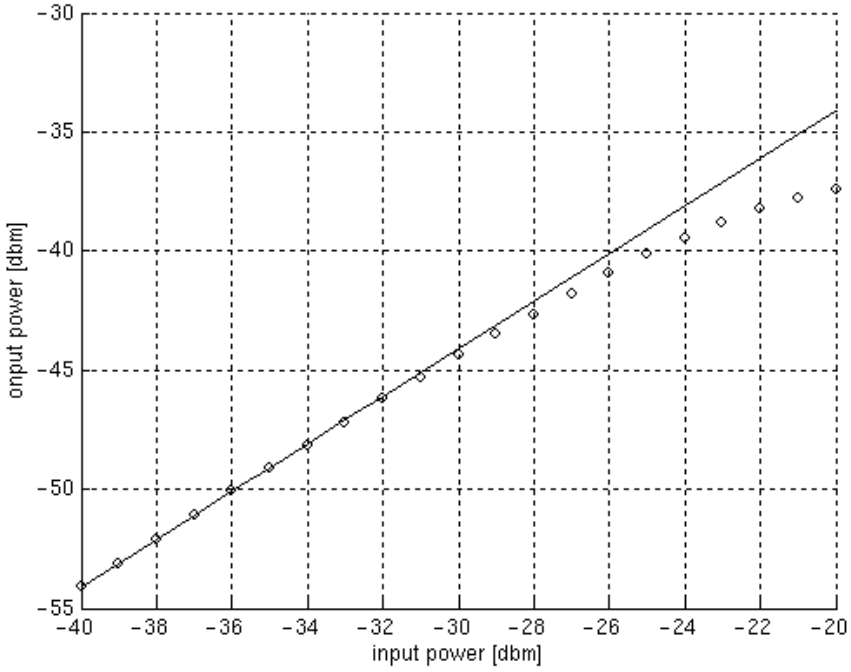


Fig. 4.24 1dB compression point measurement at f_0=1.846GHz and BW=80MHz (including the attenuation due to the buffer)

The measured output noise power (including the output buffer) is -101dBm, measured in a 1MHz resolution bandwidth, yielding 61dB of in-band dynamic range in a 1MHz RF system and 42dB of 1dB compression dynamic range. The calculated dynamic range from equation (4.26) is about 52dB for a factor gamma of 1.5. The discrepancy between the calculated and measured values is partly due to the noise contribution of the output buffer (about 2dB according to simulations), and the noise contribution of the measurement equipment itself.

The filter operates from a single 2.7V supply voltage and consumes 16mA of drain current for the previous setting. The filter can operate from a minimum power supply voltage of 2V. Table 4.3 contains a summary of filter performance parameters together with previously reported works [20,32,61] of similar filter structures. This structure offers the smallest area of all the filters reported in Table 4.3.

Table 4.3 Filter performance parameters

	[32]	**[20]**	**[61]***	**This Work**
Filter order	4	4	6	4
f_0 (GHz)	0.85	1.9	2.1	1.8
BW (MHz)	18	150	60	80
Passband gain (dB)	0	0	0	9
Ripple in passband (dB)	< ±1	+1.6	±0.35	< ±0.25
Q_{ind}	< 3	?	?	2.7
Input referred noise (dBm/Hz)	-153	-156	-155	-147
1dB compression DR	61	63	63	42
Current drain/pole (mA)	19.25	4.5	1.17+	4
Technology	0.8µm CMOS	0.25µm BiCMOS	0.25µm+ CMOS	0.5µm CMOS
Area/pole (mm^2)	0.5	0.25	0.585	0.0375
Supply voltage (V)	2.7	2.7	2.5	2.7

* No frequency programmability is provided due to usage of fixed capacitors rather than nonlinear varactors

+ Fabricated on a nonepi substrate, the current consumption increases to about 3 times if fabricated on a conventional CMOS process heavily doped epi substrate

4.7. Conclusions

A 4^{th} order tunable LC bandpass filter has been presented. The filter is fully integrated and is implemented in HP0.5µm standard CMOS process. This has the advantage of reduced silicon area, low cost, low power consumption due to the high integration level, and the elimination of extra matching elements.

A new architecture for implementing high order filters was proposed. The magnetic coupling between the inductors is emulated to provide bandwidth tuning while

maintaining small passband ripple when compared with previously published filters using on-chip transformers. The noise and linearity analyses of the filter and different design trade-offs have been demonstrated. A design strategy for maximum dynamic range was presented.

Direct tuning can be applied to tune the filter in idle time slots available in TDMA wireless standards. The information needed for both frequency and bandwidth tuning have been discussed. Measured frequency and bandwidth tuning range around 1.8GHz are 5% and 35%, respectively. The filter sinks 16mA from a 2.7V supply providing a filter bandwidth of 80MHz at 1.846GHz with a 1dB compression dynamic range of 42dB. The passband ripple is less than ±0.25dB. The filter provides a passband gain of 9dB and more than 30dB of image attenuation for an IF frequency of 100MHz.

CHAPTER V

A 100MHZ, 8MW ROM-LESS QUADRATURE DIRECT DIGITAL FREQUENCY SYNTHESIZER *

5.1. Motivation and Background

In modern wireless communication systems, fast frequency switching with fine frequency steps is crucial. Example of such systems is Bluetooth, where the signal modulation is GFSK with about 160kHz frequency deviation. Traditional PLL based synthesizer is not suitable in these applications due to the inherent loop delay. Another limitation of a PLL is the small range of frequency locking and the limited frequency resolution. Open loop voltage controlled oscillator is also not suitable due to the limited control on the output frequency.

Conventional ROM-based direct digital frequency synthesizers (DDFS), as shown in Fig. 5.1, are able to meet the above requirements by storing the values of the sine function in a ROM and scanning these values at a rate proportional to the desired frequency. The digital ROM output is converted to analog using a digital to analog converter (DAC).

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* Part of this chapter is reprinted with permission from "A 100MHz, 8mW ROM-Less Quadrature Direct Digital Frequency Synthesizer," by Ahmed N. Mohieldin, Ahmed Emira, and Edgar Sánchez-Sinencio, October 2002. *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp.1235-1243.

The main factors that determine the signal purity in this architecture are: (1) the phase quantization due to finite resolution of the phase accumulator, (2) amplitude quantization noise due to finite resolution of the DAC, and (3) static and dynamic non-idealities of the DAC. The ROM size is exponentially proportional to the desired phase resolution, resulting in huge area consumed by the ROM for reasonable phase resolutions. Moreover, the ROM should be addressed at a much higher rate than the desired output frequency for moderate spectral purities. Scanning the ROM at high speed makes it power hungry and then, unsuitable for portable wireless applications.

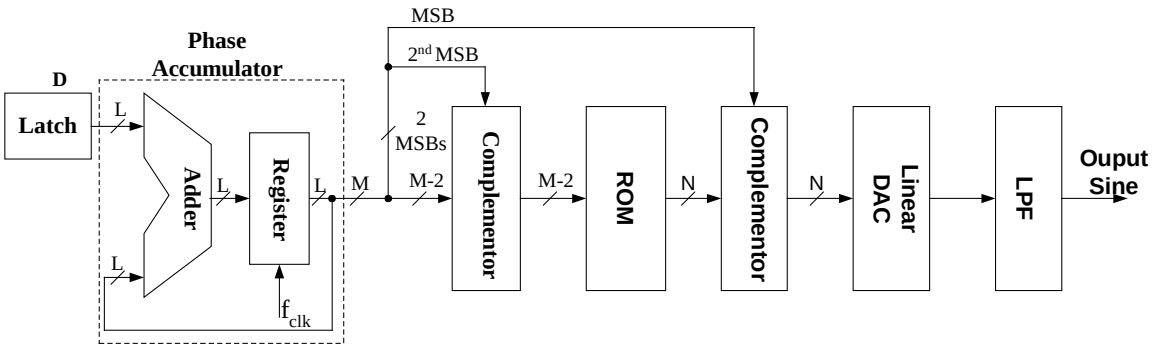

Fig. 5.1 Conventional ROM-based DDFS

Several attempts have been made to reduce the ROM size by using various techniques. The first category of solutions is based on trigonometric identities; the simplest of which is the quarter wave symmetry in the sine function (see Fig. 5.1). Other trigonometric formulas have been used to split a large ROM into two smaller coarse and fine ROMs [71]. The second category of solutions approximates the sine function over the first quarter period by another function, f(x), that can be easily implemented, as

illustrated in Fig. 5.2. In this implementation, a ROM look-up table is used to store the error, sin(x)-f(x), which results in less memory word-length requirements. The simplest form is the sine-phase difference method [72] that uses a straight-line approximation for the sine function, i.e., f(x)=x. In this scheme 2 bits of memory word-length are saved. Parabolic approximation has been also introduced [73], which results in saving 4 bits of memory word-length.

However, the above techniques are still consuming considerable area and power, hence not suitable for low cost portable applications. The third category of solutions is to use a combination of small ROM to store few sample points and a linear interpolation between these points for full computation of the generated sine function as shown in Fig. 5.3. It has been shown that this technique is efficient and the hardware cost required for the additional calculations is shown to be lower than the first two categories [74].

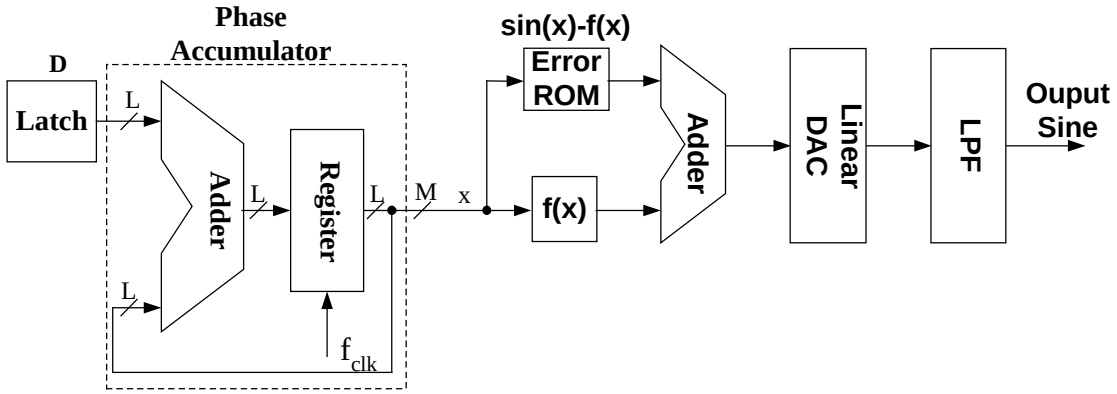

Fig. 5.2 Compression technique using approximation f(x) of the sine function

Another approach was adopted in [75] to avoid using ROM by using nonlinear DAC as shown in Fig 5.4. In this architecture, the non-linear DAC is used to achieve the

function of the phase to amplitude conversion and the digital to analog conversion at the same time. This approach was shown to provide considerable area and power savings compared to the conventional approach since the ROM is removed. There were two options for the DAC implementation.

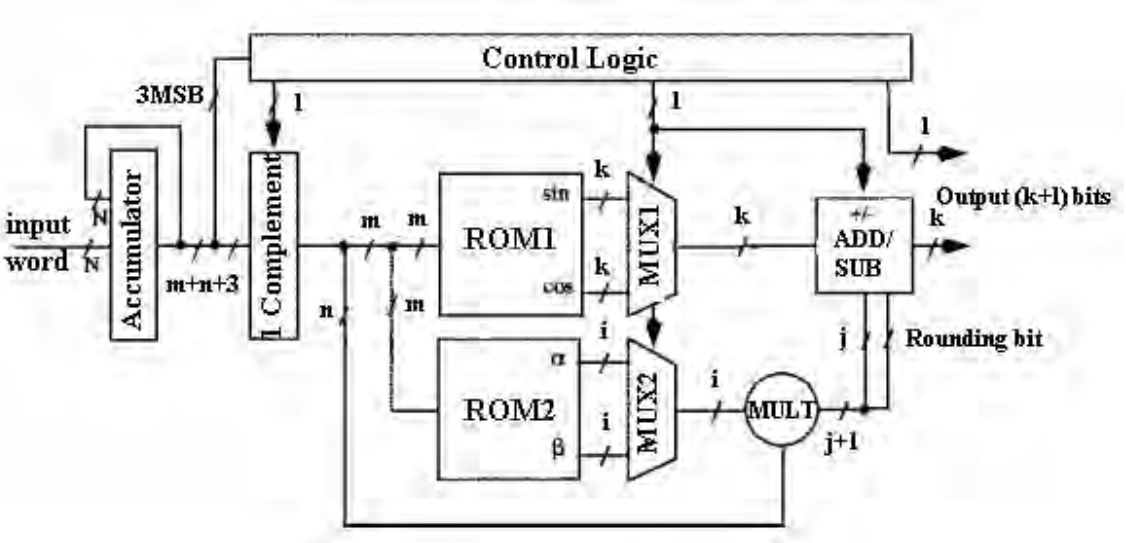

Fig. 5.3 Combining a small ROM and linear interpolation to generate sine function

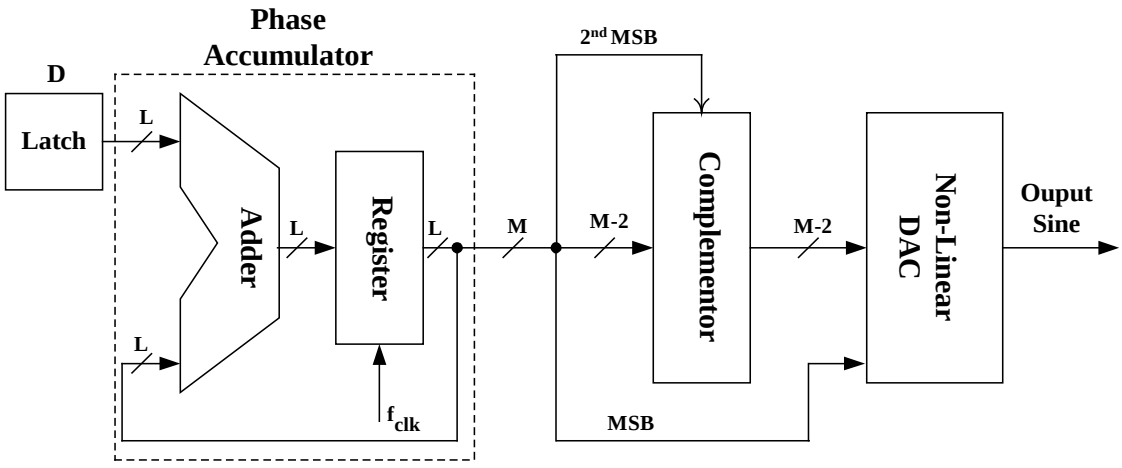

Fig. 5.4 ROM-Less DDFS using Non-Linear DAC

The first implementation is based on resistive string, which consumes less power but is inherently slow (f_{clk}=25MHz) and occupies significant area (1.7mm×1.7mm in 0.5μm technology) due to the large number of resistors and transistors used. The second implementation of the nonlinear DAC is using current-mode techniques to enhance the speed at the expense of power consumption (92mW at f_{clk}=230MHz). To further reduce the power consumption and die area, a technique was proposed in [76] to split the nonlinear DAC into a coarse DAC and a fine DAC.

In this chapter, a different approach is chosen to implement ROM-less DDFS based on piecewise linear approximation of the sine function as will be presented in the next section [77]. The proposed architecture is shown to have significant area and power savings at high clock rates. Design considerations of the building blocks will be discussed in sections 5.2-5.4. Testing results of the DDFS, as well as a comparison with recently published work, will be presented in section 5.5. Finally concluding remarks are drawn in section 5.6.

5.2. Proposed DDFS Architecture

The proposed architecture is based on the idea of breaking the sine function into linear segments as shown in Fig. 5.5, where four segments are shown for the purpose of illustration.

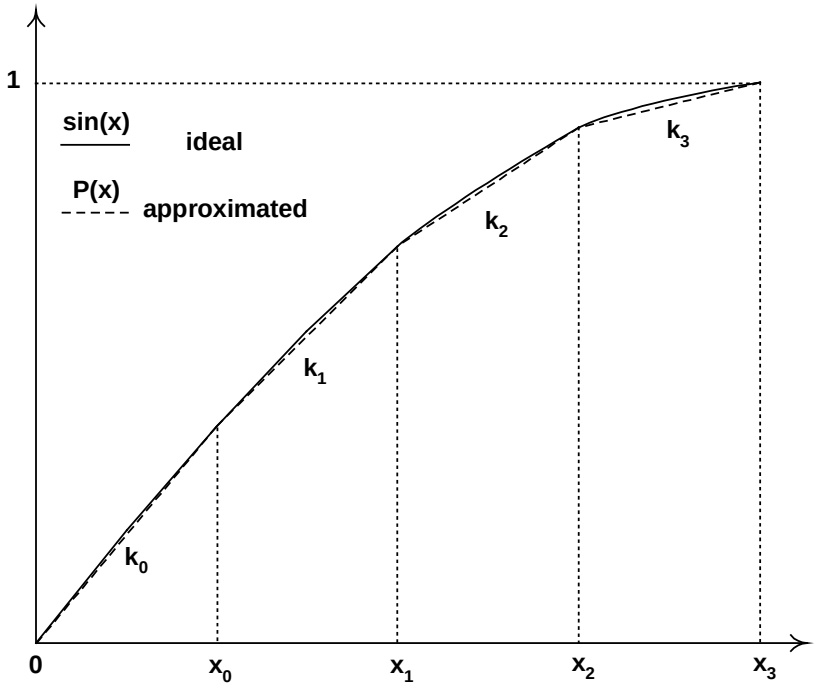

Fig. 5.5 Sine wave approximation

For a given number of segments, the segments' slopes (k_0, k1, ……) are chosen to minimize the integrated mean square error between the ideal, sin(x), and the approximate piece-wise linear, P(x), curves. In order to simplify the implementation of such approximation, the number of segments is chosen to be in powers of 2. The points X_i (i=0,1, .….) are selected to be equally spaced to further simplify the design. A MATLAB code is developed to determine the optimum set of slope values, i.e., given the number of piecewise segments, the slope values yielding *minimum mean square error* (MMSE) are determined. Where MMSE is expressed as:

$$MMSE = \min \int_{0}^{x=\frac{\pi}{2}} [\sin(x) - P(x)]^2 \, dx \tag{5.1}$$

The piecewise linear function is implemented using the block diagram shown in Fig. 5.6. The most significant M bits of the phase accumulator output are used in the phase-to-amplitude (P/A) converter. The P/A converter consists of the complementor, the linear DAC, and the switched weighted-sum (SWS) blocks. The first two MSBs of the accumulator are used to select the quarter in the sine wave cycle. The next M-2 bits are fed into the complementor, whose output is then split into two parts: α and β where α is the MSB part (a bits long), and is corresponding to the segment number, and β is the LSB part (b bits long) which is applied to the input to the DAC. For a given phase resolution (M), the proposed architecture uses an (M-2-a) bits linear DAC. Whereas, in the architecture presented in [75], an (M-2) bits nonlinear DAC is needed. Reducing the DAC bits saves significant area and promotes faster operation. The output of the SWS block is given by:

$$\begin{aligned} V_{sws} &= \sum_{n=0}^{\alpha-1} k_n V_{\min} + k_\alpha V_{DAC} + \sum_{n=\alpha+1}^{2^a-1} k_n V_{\max} && for\ E=1 \\ V_{sws} &= V_{\min} && for\ E=0 \end{aligned} \tag{5.2}$$

where V_{DAC} is the linear DAC output in the range of V_{min} to V_{max} , and E is an enable digital signal that corresponds to the positive/negative half cycle of the sine function. The SWS block in each branch implements half of the sine wave cycle, and hence the differential output voltage is a full sine wave.

The frequency of the output sine wave is given by:

$$f_{out} = \frac{D.f_{clk}}{2^L} = D.f_{\min} \tag{5.3}$$

where D is the digital accumulator input, L is the number of bits in the accumulator, f_{clk} is the input clock frequency, and f_{min} is the minimum synthesized frequency (frequency resolution) that can be obtained.

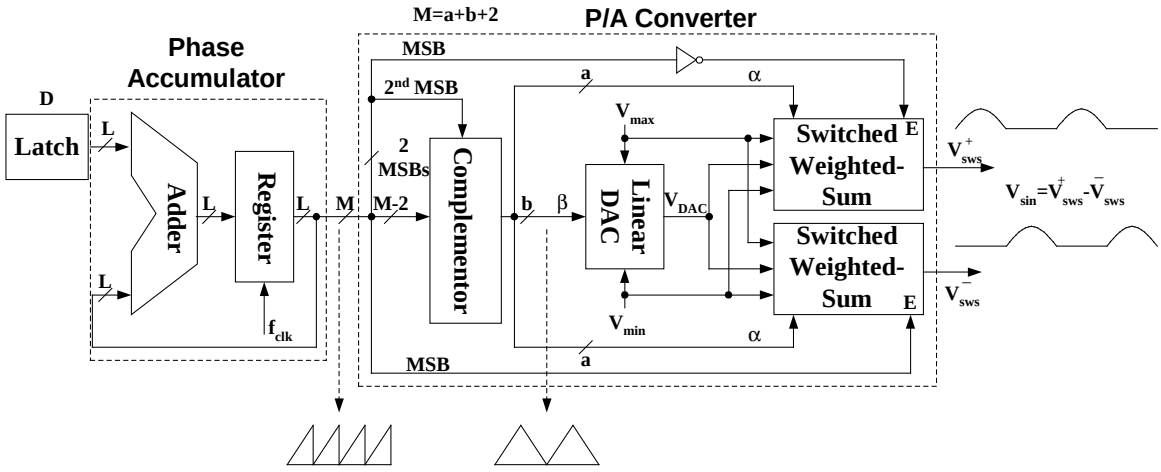

Fig. 5.6 Block diagram of the proposed DDFS architecture

In the proposed design, L=16 and f_{clk}=100MHz yielding a frequency resolution of 1.5kHz. To allow high clock rate, a 4-stages carry look-ahead adder (4 bits/stage) is used in the accumulator. Sources of distortion in the above architecture are the limited number of segments (2^a), phase resolution (M), and slope resolution. The effect of each of these parameters on the performance is simulated using MATLAB. Fig. 5.7 shows the effect of the number of segments on the spurious free dynamic range (SFDR). Note that the SFDR improves by 12 dB by doubling the number of segments. The SFDR is 59dBc and 71dBc for 8 (a=3) and 16 (a=4) segments, respectively.

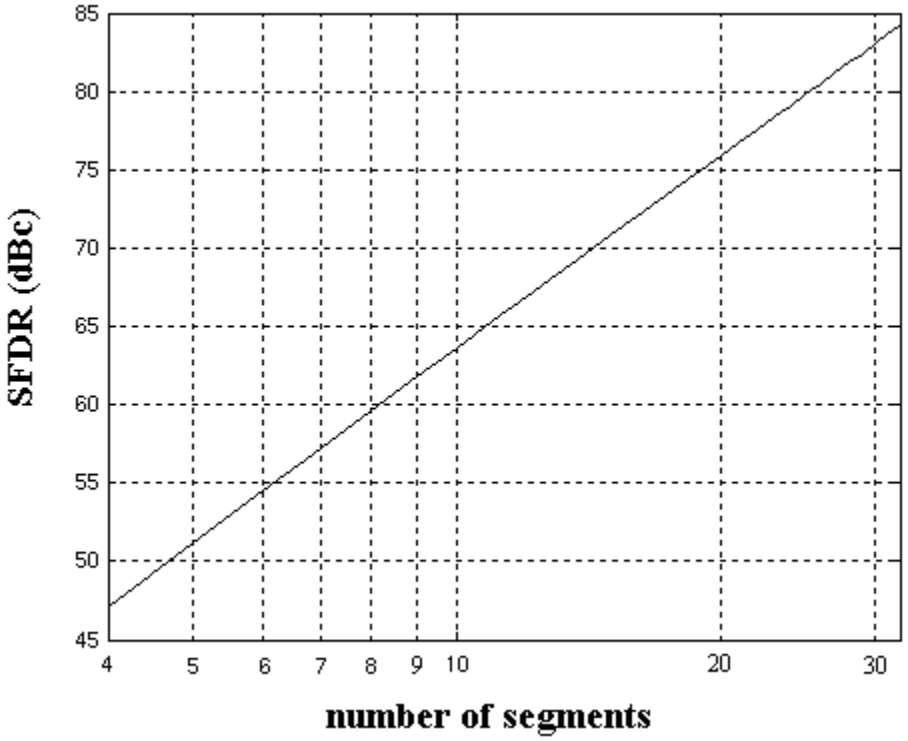

Fig. 5.7 Effect of the number of segments on the SFDR

In Bluetooth, the transmitter spurious emissions should be less than –20dBc to -40dBc at 2MHz and -40dBc to -60dBc at 3MHz, depending on transmitter power class. Since the 16-segments DDFS consumes about 50% more power and area than the 8-segments design, as will be shown at the end of section 4, 8-segments design is adopted. A passive RC pole can be used at the DDFS output to attenuate the spurs at frequencies far from the fundamental output. For 8 segments, the effect of the finite phase resolution is shown in Fig. 5.8. It shows that no significant improvement in the SFDR is achieved for phase resolutions more than 10 bits. For this choice of M=10 and a=3, only 5-bit DAC (b=M-2-a=5) is needed.

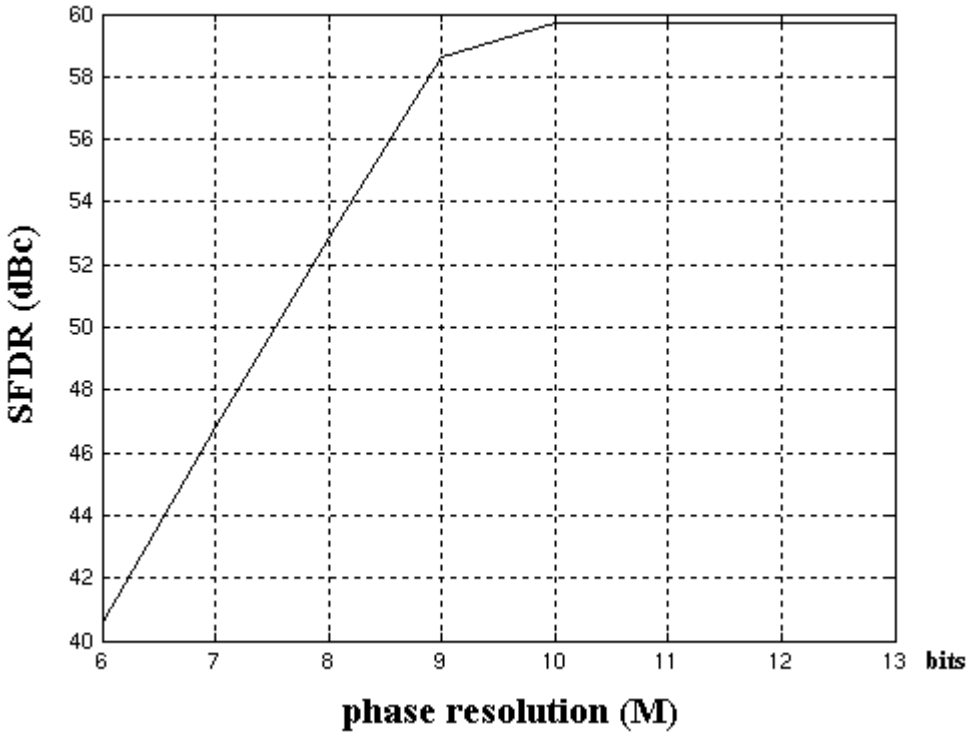

Fig. 5.8 Effect of phase resolution on the SFDR

The weighted-sum function is implemented using resistive dividers (as will be discussed later). Each resistance is an integer multiple of a unit resistance ΔR, which determines the slope resolution. The effect of finite unit resistance is shown in Fig. 5.9 for 8 segments and 10 bits of phase resolution.

Note that for a normalized unit resistance ($\Delta R/R_{max}$) less than 0.4%, there is no much improvement in SFDR. To allow for some margin, ($\Delta R/R_{max}$)=0.2% is a good choice for an 8 segment sine shape. An extra care must be taken in the layout of these resistors to achieve the required resolution.

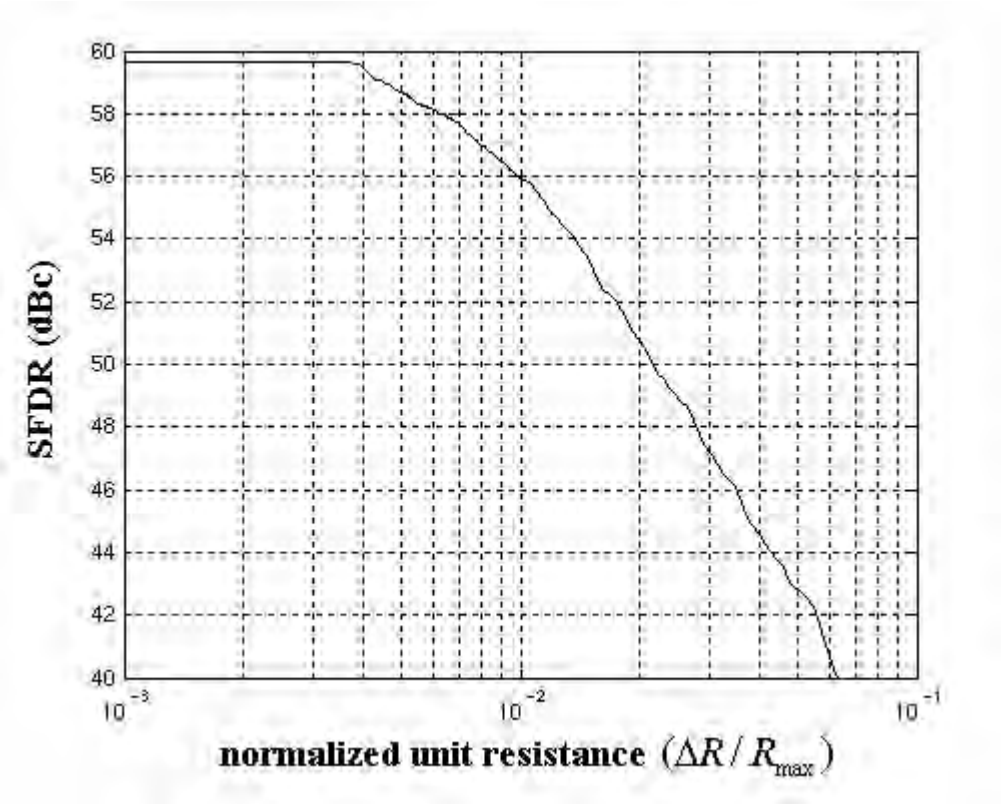

Fig. 5.9 Effect of finite unit resistance on the SFDR

Table 5.1 summarizes the required values of phase resolution (M), normalized unit resistance, and the corresponding SFDR for different number of segments. Note that doubling the number of segments, i.e., increasing (a) by 1 requires 2-bit increase in the phase resolution. This implies doubling the size of the linear DAC, i.e., increasing (b) by 1.

Quadrature outputs are generated by replicating the P/A converter. The 90^0 phase shift is implemented by adding 01 to the two MSBs of the accumulator output.

Table 5.1 Required values of (M), ($\Delta R/R_{max}$), and corresponding SFDR for different number of segments

Number of segments	Phase resolution (M)	($\Delta R/R_{max}$)	SFDR
4	8 bits	0.7 %	47 dBc
8	**10 bits**	**0.4 %**	**59 dBc**
16	12 bits	0.2 %	71 dBc
32	14 bits	0.1 %	83 dBc

5.3. Linear DAC

The 5-bit resistive string DAC is implemented as shown in Fig. 5.10. In order to have smoother transitions at the corner points between segments in the output sine wave, a ½ LSB offset is introduced to the DAC output by using R/2 value for the lower and uppermost resistors. A 5-to-32 decoder is used to turn ON the switch corresponding to the digital input β. At any given time, only one switch must be turned ON. Due to non-equal delays at the decoder outputs, more than one switch can be turned ON at the same time or all the switches can be turned OFF. This will result in undesirable glitches at the output of the DAC. To solve this problem, the outputs of the decoder are sampled at $\overline{CLK}$.

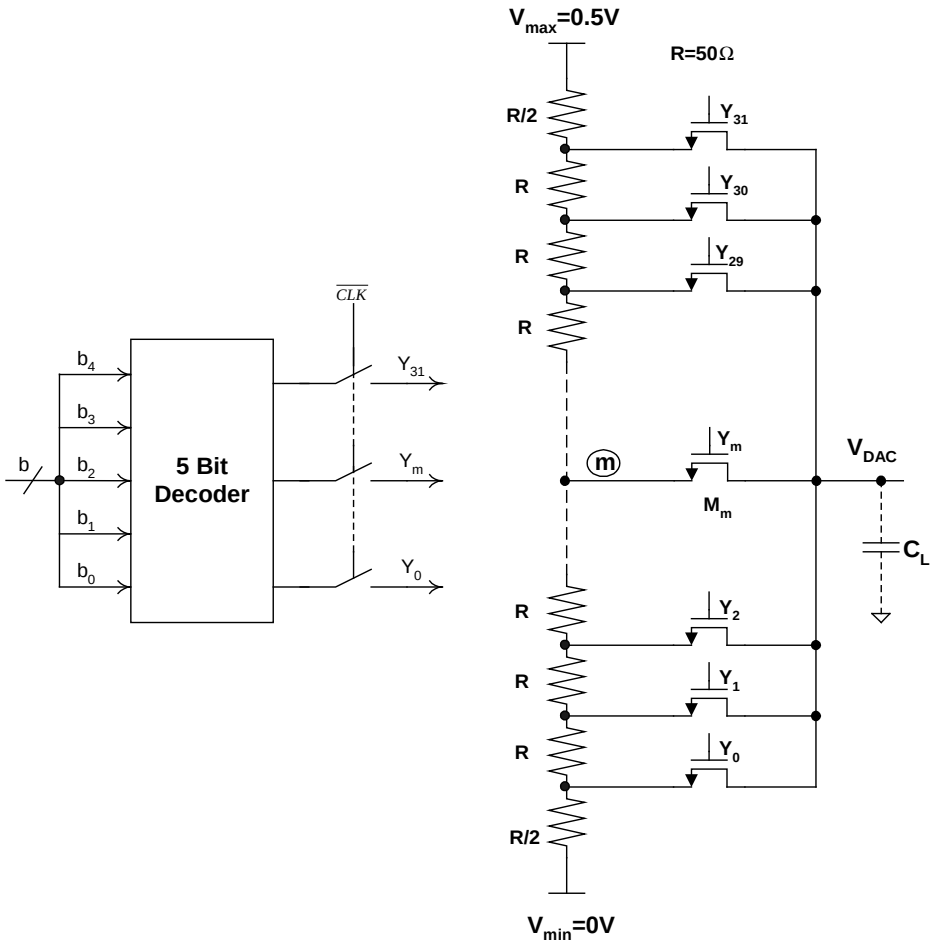

Fig. 5.10 Linear DAC circuit implementation

The settling time for each digital input word is determined by three factors: (1) The total capacitance (C_L) at the output node V_{DAC} which is dominated by the drain capacitances of all the switches and the input capacitance of the next stage. (2) The input resistance of the resistive string seen from the corresponding node (m). The closer the node to the middle of the resistor string, the higher the resistance seen. The value of R is chosen as a trade-off between power consumption and settling time. For this particular design, R=50Ω is found to be a good compromise. (3) The ON resistance, R_{ON}, of the

corresponding switch M_m. In order to minimize the load capacitance C_L, different transistors' widths are used to have the same settling time for all digital input combinations. To allow for large overdrive voltage in the NMOS switches, the terminal voltages (V_{min} and V_{max}) of the resistor string are chosen to be 0V and 0.5V, respectively.

5.4. Switched Weighted-Sum Block

Two SWS blocks are used in the system, one for each half of the sine wave cycle. The details of the SWS block are shown in Fig. 5.11.

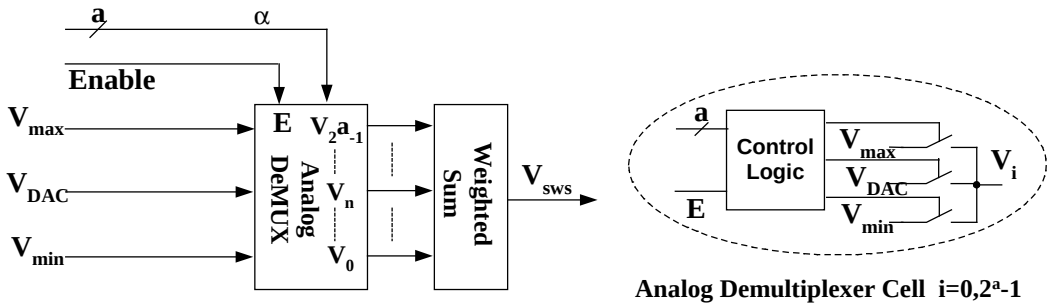

Fig. 5.11 Switched weighted-sum block

The output of the SWS block can be written as:

$$V_{sws} = \sum_{n=0}^{2^a-1} k_n V_n \tag{5.4}$$

The role of the analog demultiplexer is to route V_{max}, V_{DAC}, or V_{min} to V_n based on the value of α, corresponding to the segment number, and enable E as follows:

$$\begin{aligned} V_n &= V_{\max} \quad for \;\; n<\alpha \;\; \& \;\; E=1 \\ V_n &= V_{DAC} \quad for \;\; n=\alpha \;\; \& \;\; E=1 \\ V_n &= V_{\min} \quad for \;\; n>\alpha \;\; \& \;\; E=1 \\ V_n &= V_{\min} \quad for \;\; E=0 \end{aligned} \tag{5.5}$$

The analog demultiplexer consists of 2^a cells, one for each output. The basic analog demultiplexer cell for each output V_i for i=0,2^a-1 is illustrated in the same figure.

The weighted-sum function described in equation (5.4) is implemented using resistors and buffers as shown in Fig. 5.12. Assuming ideal buffers (unity gain and zero output resistance), the weighted-sum output V_{sws} is given by:

$$V_{sws} = \frac{\sum_{n=0}^{2^a-1}(V_n / R_n)}{\sum_{n=0}^{2^a-1}(1/R_n)} = \frac{\sum_{n=0}^{2^a-1}(V_n / R_n)}{G_T} \tag{5.6}$$

where $R_T=(1/G_T)$ is the parallel combination of all resistors in the weighted-sum network. Comparing equations (5.4) and (5.6), we get:

$$k_n = \frac{R_n}{R_T} \qquad n = 0,1,\cdots,2^{a-1} \tag{5.7}$$

Equation (5.7) is used to obtain the values of R_n from the segments' slopes. Note from equation (5.6) that V_{sws} depends on the ratio of resistors, hence the matching of the resistors in the weighted-sum block in each branch is a critical issue. On the other hand, matching between the resistors of the weighted-sum blocks in both positive and negative branches is not critical.

The buffers are the most power consuming parts in the proposed system. Care must be taken in the design of these buffers to minimize the overall power consumption while keeping good linearity.

Fig. 5.12 shows also the transistor level design of each buffer. PMOS input transistors are used to eliminate the body effect by shorting the source and body terminals (nwell technology is used). Another advantage of using PMOS input transistor is that the input voltage can be as low as 0V. Since this voltage is routed from the DAC resistor string to the buffer input using MOS switches (in the DAC and the analog demultiplexer), then fast NMOS switches can be used with high overdrive voltage. This helps to minimize the delay associated with these switches without having to use wide transistors. Note that the output voltage of each buffer is DC shifted by V_{SG} relative to its input. Since all the buffers are biased using the same biasing voltages V_{B1} and V_{B2}, they all have the same nominal DC shift. However, due to mismatches between transistors in different buffers, this DC shift may differ from one buffer to the other. These DC shift mismatches will result in a slight offset in the output sine wave, but will not affect its spectral purity.

Since buffers have different load resistances, the actual relative slope values of the segmented sine wave will be slightly different from equation (5.7) if the buffers were identical due to of the finite buffer output resistance. One way to dilute this effect is to reduce the buffers output resistance by increasing the bias current or increasing W/L of M_1 (Fig. 5.12), which will increase the power consumption or increase the load capacitance to the analog demultiplexer, respectively.

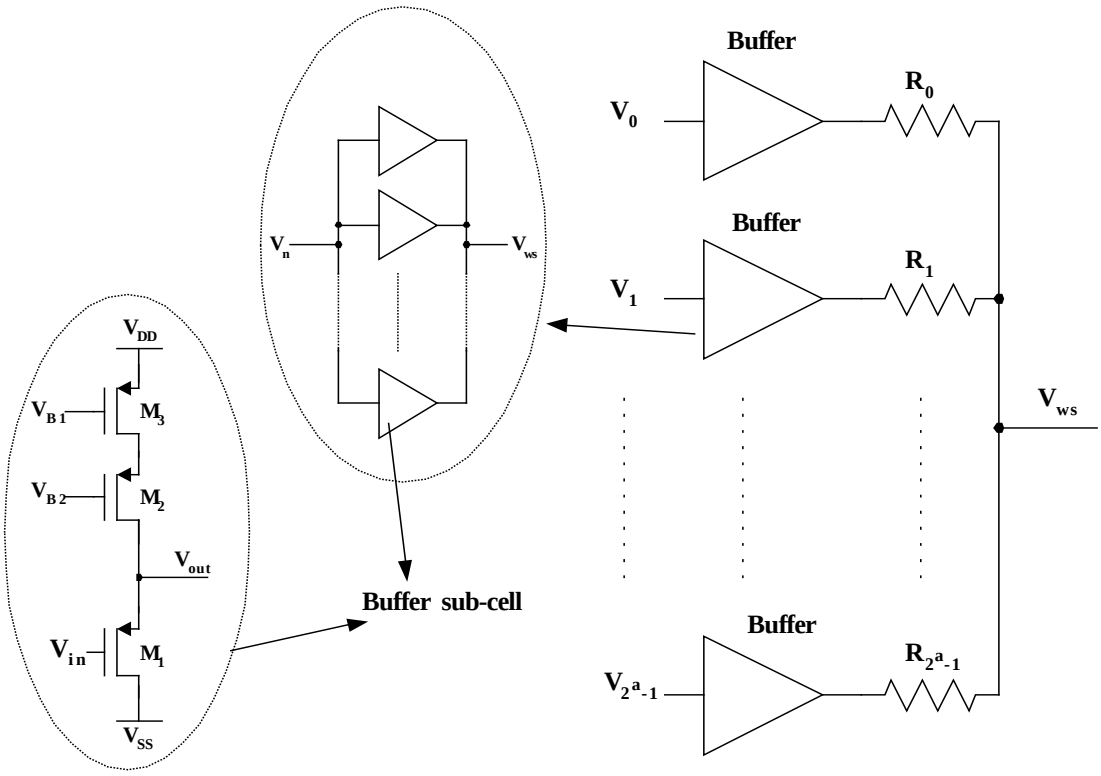

Fig. 5.12 Implementation of the weighted-sum block

Instead, to have the same loading effect on all buffers, each buffer is designed such that the ratio of its output resistance to the load resistance is the same for all buffers. To allow better matching between buffers, each buffer is designed as a number of parallel buffer sub-cells. These sub-cells are identical in all buffers, but the number of parallel sub-cell in each buffer is inversely proportional to the desired output resistance. As a result, the buffers' output resistances will account for a slight attenuation, but the relative slope values of the segments remain unchanged. Consequently, the total current drain in all buffers will be inversely proportional to the parallel combination, R_T, of all resistors in the weighted-sum network. Hence, scaling of all resistors is very important in

determining the overall power consumption. However, the higher the value of R_T, the slower the response of the circuit due to the large time constant R_TC, where C is the input capacitance of the following stage. The settling error within the clock period is given by:

$$settling\ error = \Delta V_{out} e^{-\frac{1}{f_{clk} R_T C}} \tag{5.8}$$

The largest error corresponds to the largest output voltage step $\Delta V_{\max} = 0.5V$. This largest error should be set to be smaller than the smallest output step, which corresponds to the smallest slope. For the particular case when a=3, the smallest slope value (obtained from the MMSE algorithm implemented in MATLAB) is 0.096 for a sine wave of unit amplitude. Therefore, the smallest output step is:

$$smallest\ output\ step = \Delta V_{\min} = DAC\ step \times smallest\ slope = \frac{0.5}{2^5} \times 0.096 = 1.5mV \tag{5.9}$$

By fixing the settling error in equation (5.8) smaller than the above value, we get:

$$R_T < \frac{1}{C.f_{clk} \ln\left(\frac{\Delta V_{\max}}{\Delta V_{\min}}\right)} = \frac{1}{5.81C.f_{clk}} \tag{5.10}$$

The value of C determines the integrated output noise due to resistors, known as KT/C noise. This noise should be sufficiently smaller than the largest output spur, which in this case is 59dB below the fundamental tone. If we set the noise level to be lower than this spur, then:

$$\sqrt{\frac{KT}{C}} < \frac{A}{\sqrt{2}\ 10^{(SFDR/20)}} \tag{5.11}$$

where, K is Boltzmann constant, T is the temperature (assumed 300°K), and A is the output amplitude (0.5V).

In case of 8 segments approximation, the above equation yields C > 0.026pF. This is rather a loose condition for this capacitance, which is typically larger than 0.1pF. In this design, 0.3pF is assumed for the load capacitance, for which the maximum parallel resistance R_T is 5.7kΩ, as given by equation (5.10) for f_{clk}=100MHz. To allow for some margin for process variations, all resistances are scaled to have a nominal parallel combination of 3kΩ. The lowest and highest resistors in the weighted sum network are 15kΩ and 150kΩ, respectively.

An alternative switched capacitor implementation of the weighted-sum block is shown in Fig. 5.13. The period of the two phases φ_1 and φ_2 is $(0.5/f_{clk})$. Since the phases φ_1 and φ_2 are non-overlapping phases, the period should be chosen less than $(0.5/f_{clk})$. The weighted-sum output V_{sws} is given by:

$$V_{sws} = \frac{-1}{C_F} \sum_{n=0}^{2^a-1} C_n V_n \tag{5.12}$$

Equation (5.12) is valid for phase φ_1, while the output is hold by capacitor C_H during φ_2. Comparing equations (5.4) and (5.12), we get:

$$k_n = \frac{C_n}{C_F} \qquad n = 0,1,\cdots,2^{a-1} \tag{5.13}$$

Equation (5.13) is used to obtain the values of C_n from the segments' slopes. Note from equation (5.13) that V_{sws} depends on the ratio of capacitors, hence the matching of the capacitors in the weighted-sum block in each branch is a critical issue. On the other

hand, matching between the resistors of the weighted-sum blocks in both positive and negative branches is not critical.

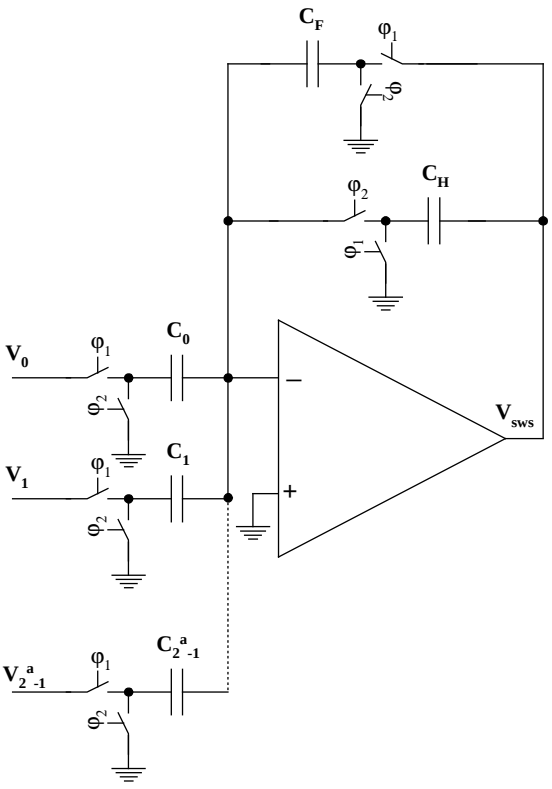

Fig. 5.13 Alternative implementation of the weighted-sum block

Example. The minimum value of the capacitor C_{min} is determined by the noise requirement, which should be sufficiently smaller than the largest output spur. For the case of 8 segments the integrated noise should be 59dB below the fundamental tone. According to equation (5.11) this results in a C_{min} of 0.3pF.

Because of the finite GBW of the OpAmp, the output voltage will not settle to its final value during φ_1. To make this error negligible, it is required, as a rule of thumb, that:

$$m.GBW.T>5 \tag{5.14}$$

where m is the capacitor ratio between the sum of all the feedback capacitors divided by the sum of all the capacitors connected to the input terminal of the Op Amp, and T is the period of the clock frequency. In our case, m=1/5 according to equation (5.13). Thus, from equation (5.14) and for f_{clk}=100MHz, GBW should be larger than 2.5GHz.

$$GBW > 2.5\times10^9 \Rightarrow \frac{g_m}{2\pi C_{\min}} > 2.5\times10^9 \Rightarrow \frac{I_{tail}}{2\pi V_{ov} C_{\min}} > 2.5GHz \tag{5.15}$$

A value of V_{ov}=0.5V and C_{min}=0.3pF results in a tail current of the input stage of the OpAmp I_{tail} of 2.4mA. Due to the finite gain of the OpAmp, the steady state settling value deviates from its ideal value. To minimize this error, the gain of the OpAmp should be at least 60dB, which might require a two-stage OpAmp. This makes the design more difficult in terms of stability requirements, i.e., phase margin. For the OpAmp to act as a single pole system with enough phase margin, the frequency of the non-dominant pole ω_{nd} must be pushed at least twice that of GBW, i.e., ω_{nd} > 5Grad/sec. In the used technology (0.5μm process), this means even pushing more current than calculated previously, i.e., I_{tail}. The current consumption of the first solution of the weighted sum block, shown in Fig. 5.12, is 1.5mA as shown in section 5. Since the current consumption of the second solution, shown in Fig. 5.13, is more than 2.4mA, the first solution has been adopted in the final design.

Design Procedure. A simple design strategy for the proposed DDFS architecture, for a given SFDR, can be itemized as:

1. Choose the number of segments of the piecewise linearly approximated sine function according to Fig. 5.7 for the required SFDR.
2. The values of the slopes of the piecewise linearly approximated sine function are calculated to minimize MMSE as given by equation (5.1)
3. The required values of phase resolution (M) and resistance mismatch ($\Delta R/R_{max}$) are calculated from Table 5.1.
4. Calculate the value of C such that the integrated output noise, i.e. KT/C noise, is sufficiently smaller that the largest output spur as given by equation (5.11).
5. Calculate the value of the maximum parallel resistance R_T such that the settling error is smaller than the minimum output step, ΔV_{min}, for the used clock frequency f_{clk}.

Example. Consider the case of 16 segments (a = 4). The targeted SFDR is 71dB and the smallest slope is 0.05. According to Table 5.1, the minimum phase resolution for 71dB SFDR is 12bits. Hence, the number of DAC bits is $b = M - 2 - a = 6$. From equation (5.11), we get C > 0.42pF. If we take C = 0.5pF (this may require adding a physical capacitance), then the parallel combined resistance will be $R_T < 2.8k\Omega$. If we choose $R_T = 2k\Omega$, this design will consume about 50% more power compared to the 8-segments design. The buffers' area will roughly increase by the same percent.

5.5. Measurement Results

The proposed quadrature (I & Q) output DDFS has been implemented through MOSIS, in 0.5μm AMI CMOS process. The die photo is shown in Fig. 5.14. The chip active area is 1.4mm^2, of which 25% is occupied by the phase accumulator.

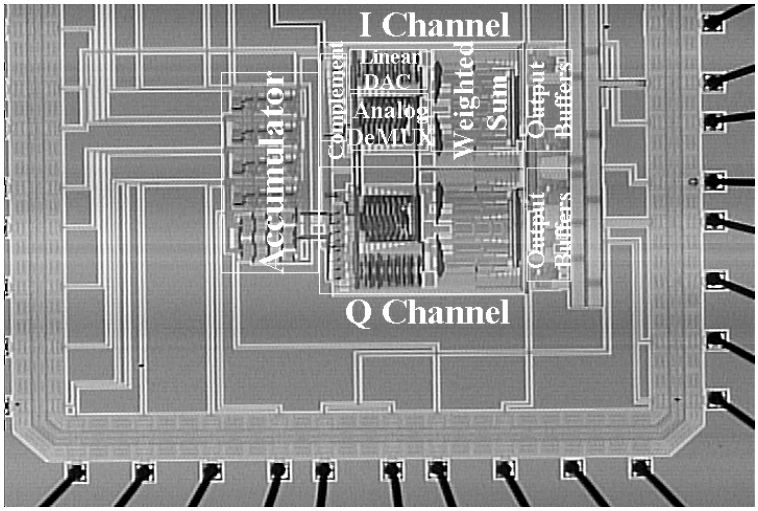

Fig. 5.14 Chip micrograph

On-chip buffers are included to drive the pin capacitance. The DDFS operates from a single 2.7V supply with 3mA current drain and a clock frequency of 100MHz. The testing setup incorporates an off-chip instrumentation amplifier, as shown in Fig. 5.15, for differential to single-ended conversion. It uses low distortion (THD=-75dB at 1MHz) buffer amplifiers with 1pF input capacitance.

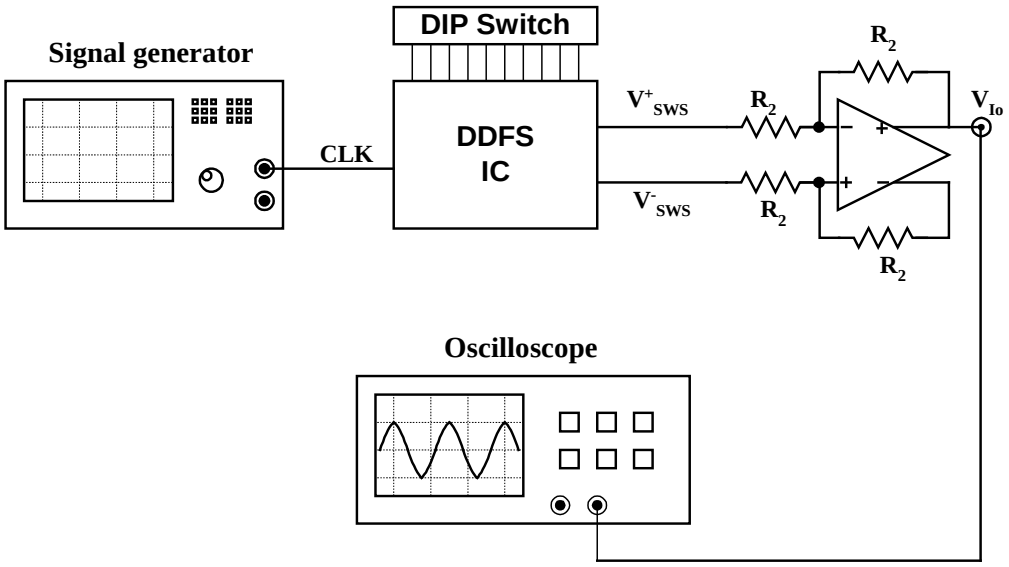

Fig. 5.15 Testing setup

Fig. 5.16 shows the single-ended outputs ($V_{sws}^{+}$and V_{sws}^{-}) of the I branch as well as the differential output when f_{out}=98kHz. Fig. 5.17 shows the two quadrature outputs of the I & Q branches at the same output frequency. The peak-to-peak magnitude is about 910mV, which is slightly less than the ideal $1V_{p-p}$ magnitude due to the expected attenuation of the weighted-sum and the output buffers.

The modulation capabilities of the proposed DDFS have been also tested. Fig. 5.18 shows an example of frequency modulation where the modulating signal is a square wave of frequency 1kHz. An example of amplitude modulation is shown in Fig. 5.19. The modulating signal is applied at V_{max} (see Fig. 5.9). It is a sine wave of frequency 1kHz and peak-to-peak magnitude of 400mV with a DC offset of 250mV.

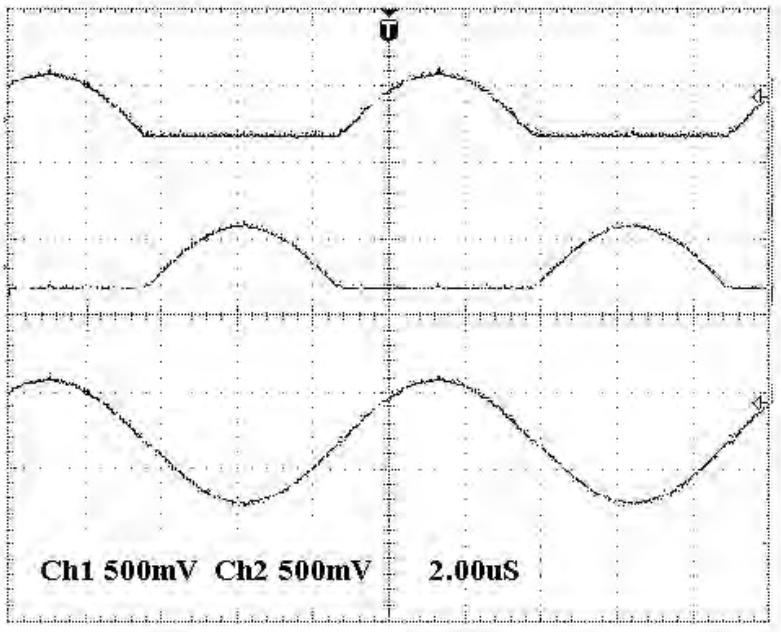

Fig. 5.16 Single-ended and differential outputs of the I branch (f_{out}=98kHz)

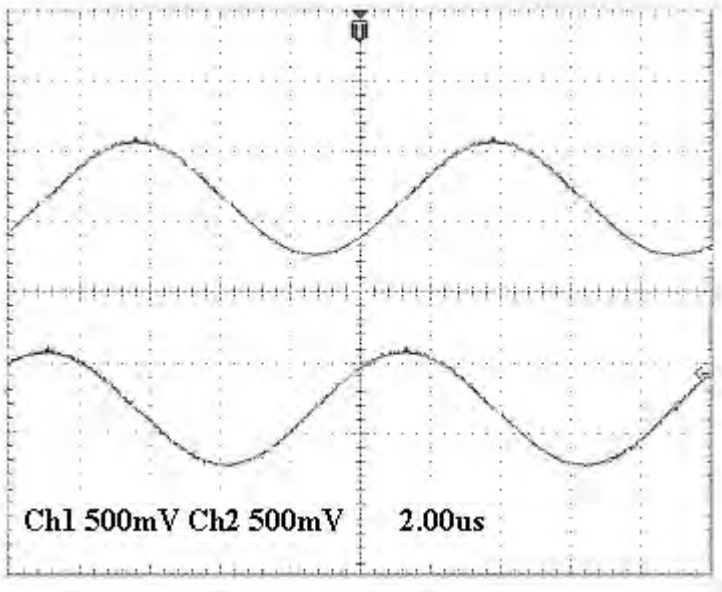

Fig. 5.17 Quadrature outputs I and Q at f_{out}=98kHz

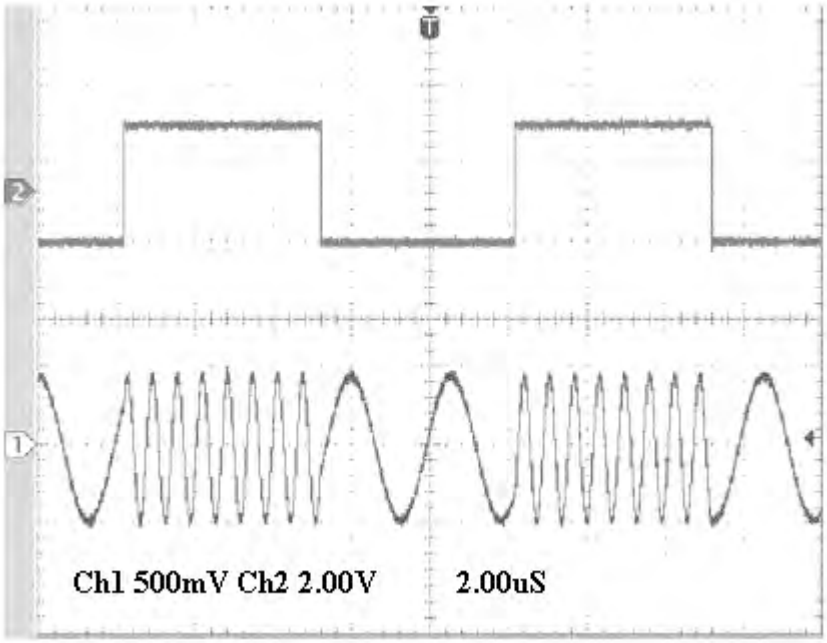

Fig. 5.18 Frequency modulation

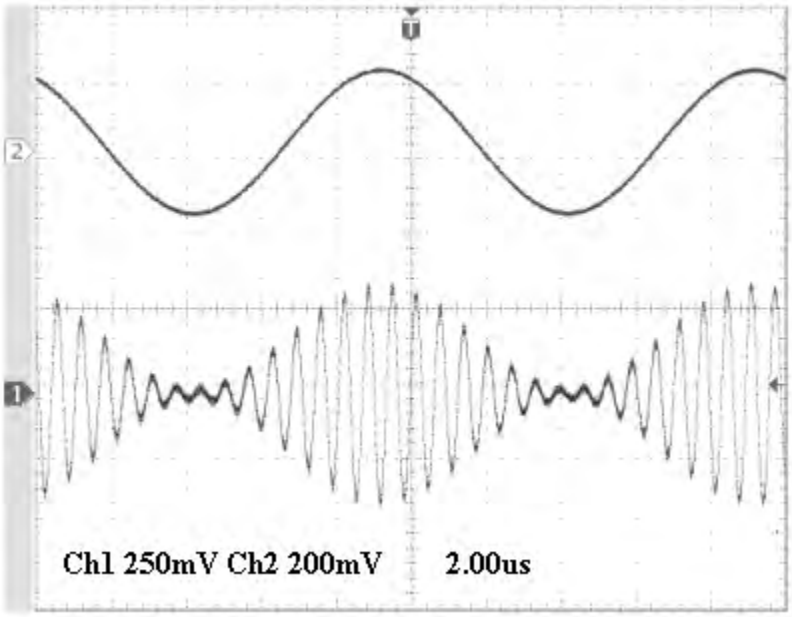

Fig. 5.19 Amplitude modulation

The output spectrum for $f_{out}=(f_{clk}/1024)=98kHz$ and $f_{out}=(f_{clk}/64)=1.56MHz$, at which the SFDR is 57.3dBc and 42.1dBc, are shown in Fig. 5.20 and Fig. 5.21 respectively.

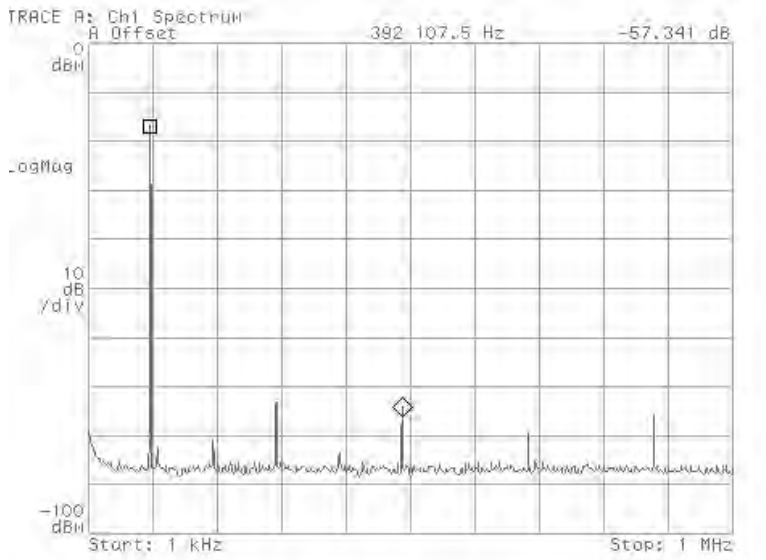

Fig. 5.20 Output spectrum at $f_{clk}=100MHz$ and $f_{out}=98kHz$ with SFDR=57.3dBc

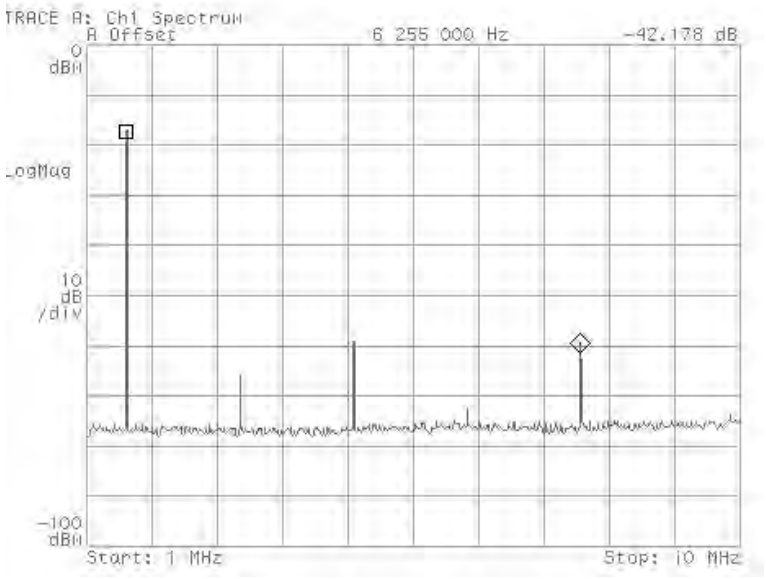

Fig. 5.21 Output spectrum at $f_{clk}=100MHz$ and $f_{out}=1.56MHz$ with SFDR=42.1dBc

The SFDR versus the output synthesized frequency is plotted in Fig. 5.22. The SFDR is better than 59dBc for low synthesized frequencies. For high synthesized frequencies, the SFDR is degraded due to large output steps of the DAC and the switched weighted-sum blocks. Fig. 5.23 shows the SFDR versus the clock frequency for $f_{out}=(f_{clk}/128)$.

The DDFS is shown to operate from a clock frequency up to 130MHz. Higher clock frequencies could not be achieved due to the frequency limitations of the phase accumulator.

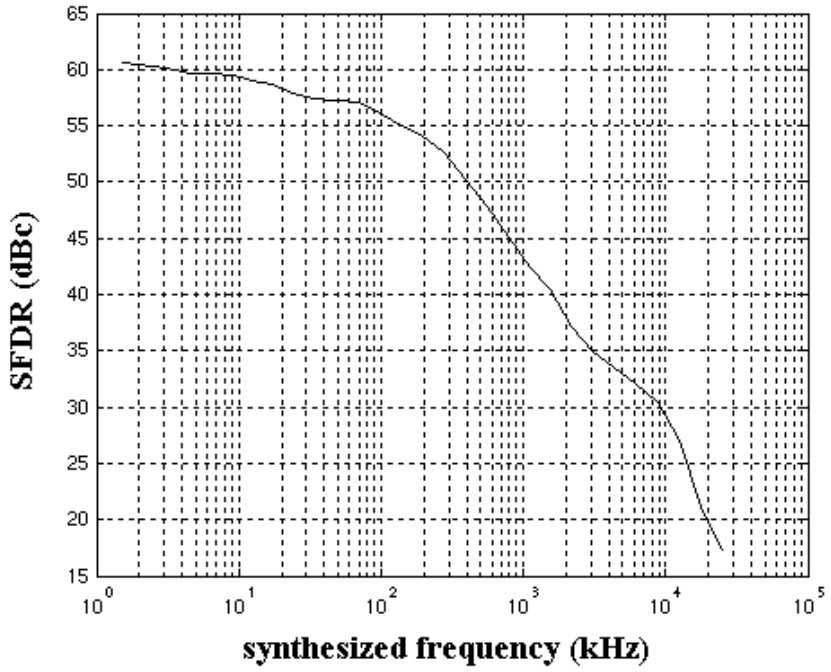

Fig. 5.22 SFDR versus synthesized frequency at f_{clk}=100MHz

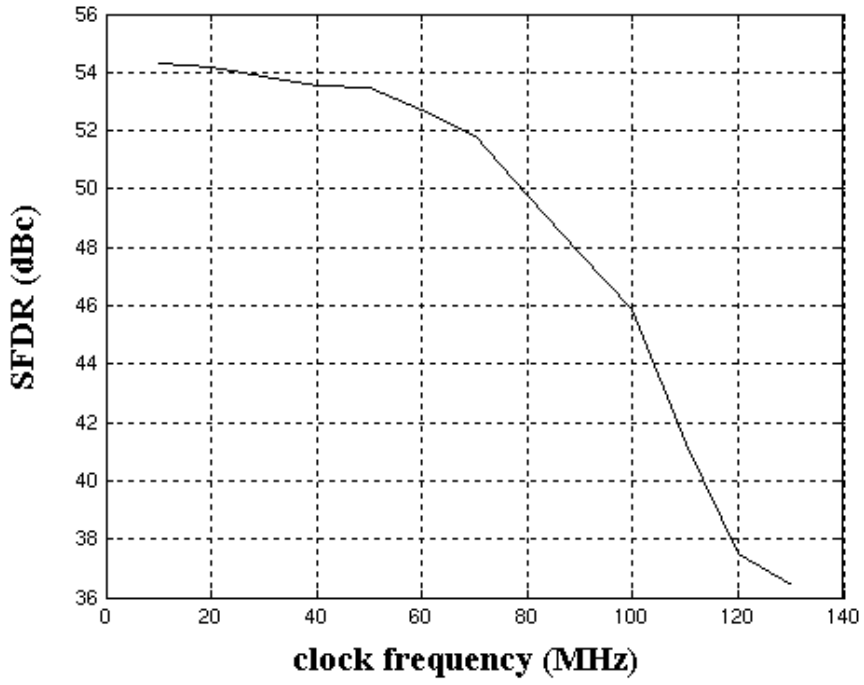

Fig. 5.23 SFDR versus clock frequency at $f_{out}= f_{clk}/128$

The proposed DDFS is compared with the recently reported synthesizers [74-76] as listed in Table 5.2. Note that the DDFS presented in [74] does not have an On-chip DAC and the DDFS presented in [76] does not have quadrature outputs. The energy of the proposed DDFS (in mW/MHz) is significantly lower than state-of-the-art implementations due to the removal of the ROM and the small DAC size. Therefore, the proposed design is more suitable for low power portable applications. A better SFDR can be achieved, using the proposed architecture, by doubling the number of segments (a=4). This can increase the SFDR by 12dB at the expense of increasing the power consumption and active area by roughly 50% and 40%, respectively.

Table 5.2 Comparison with recently published work

	[74]	**[75]**	**[76]**	**This Work**
Clock frequency (MHz)/ Operating frequency (kHz)	30 1560	230 200	300 4000	100 200
Phase resolution (bits)	12	10	12	10
Technology (μm CMOS)	0.8	0.5	0.25	0.5
Quadrature outputs	Yes	Yes	No	Yes
On-chip DAC	No	Yes	Yes	Yes
Power dissipation (mW)	9.5	92.5	240	8
Power supply (V)	3.3	3.3	2.5	2.7
SFDR (dBc)	60	55	62	59
Active area (mm^2)	0.9	1.6	1.4	1.4
Energy (mW/MHz)	0.3	0.4	0.8	0.08

5.6. Particular Case

The conventional direct digital synthesizer, i.e., ROM based, can been used to provide sawtooth and ramp waveforms as presented in [78]. The same is applies for the proposed DDFS. This is the case because the proposed DDFS share the same front end as the conventional DDFS. The front end is composed of a digital part (the phase accumulator and the complementor) followed by a D/A converter, as shown in Fig. 5.24. Please note that the frequency of the saw-tooth and triangular waveforms, shown in Fig. 5.24, is $4f_{out}$ and $2f_{out}$, respectively, where f_{out} is defined in equation (5.3). The peak of the triangular wave after the linear DAC is V_{max}, while the slope is 1.

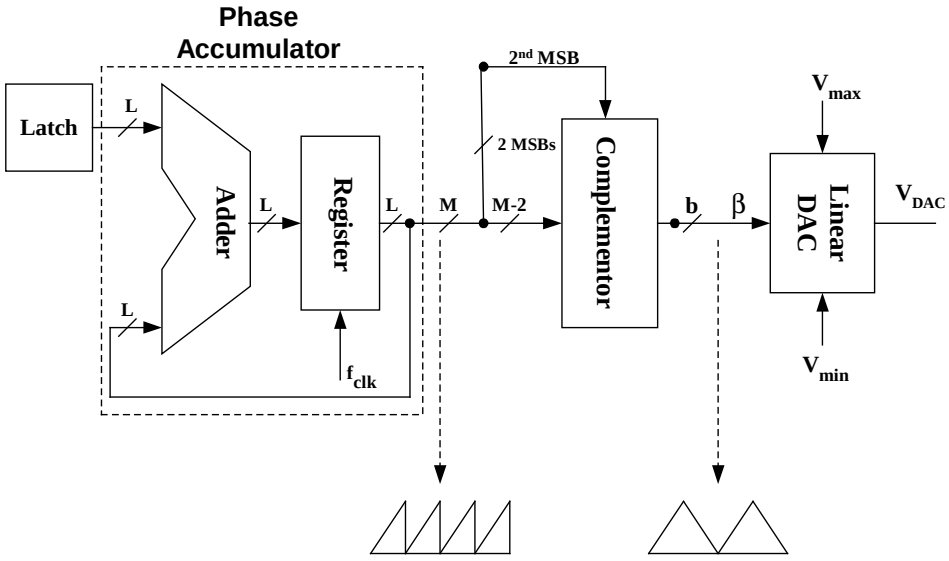

Fig. 5.24 Front end of DDFS

One of the possible applications of using the ramp function is in built-in self testing (BIST) [79]. The basic requirement in those kinds of applications is the accuracy of the ramp waveform. This translates directly to the accuracy of the DAC in Fig. 5.24 since the digital part does not play any role in the distortion of the waveform. Many DAC architectures have been reported in the literature [48]. For the resistor string approach, discussed in section 5.3, the accuracy depends on the matching precision of the resistors. Using polysilicon resistors can result in up to 0.1%, i.e., 10 bits of accuracy. This might not be enough for some applications. Dynamic techniques with current switching can be used to realize D/A converters with higher accuracy (up to 16 bits) [48].

5.7. Conclusions

A low-power ROM-less quadrature DDFS architecture has been presented. It uses a piecewise linear approximation of the sine function. The proposed DDFS has been implemented in 0.5μm CMOS technology and occupies an area of 1.4mm^2. A 16-bit frequency control word results in a tuning resolution of 1.5kHz at a 100MHz clock frequency.

The proposed design operates from a single 2.7V supply while consuming 8mW. The design features an SFDR that is better than 50dBc for synthesized frequencies up to $f_{clk}/256$. The proposed architecture also incorporates different modulation capabilities. The modulation formats include frequency modulation and amplitude modulation. Since the proposed design consumes significantly less power than recently reported designs, it is a good candidate for wireless portable communication applications that use frequency modulation such as Bluetooth and GSM.

There are two frequency limitations in this design. First, higher clock frequencies are limited by speed of the phase accumulator. Digital techniques can be used to solve this problem [75]. Using better process, i.e. smaller feature size, improves the speed of digital blocks such as the accumulator. Second, higher synthesized frequencies are limited by the settling time of the DAC due to large output steps. The values of the resistors in the DAC can be reduced to improve the settling time at the expense of power consumption.

For applications that require higher SFDR, the number of linear segments can be increased at the expense of area and power consumption. For example, doubling the

number of segments increases the SFDR by 12dB at the expense of increasing the power consumption and active area by roughly 50% and 40%, respectively. The proposed architecture can be also used to generate triangular and/or saw-tooth waveforms, as shown in Fig. 5.6, using an extra DAC and a smoothing low pass filter.

CHAPTER VI

A 2V 11 BITS INCREMENTAL A/D CONVERTER USING FLOATING GATE TECHNIQUE

6.1. Motivation and Background

As the feature size of modern CMOS processes scales down, the maximum allowable power supply continuously decreases and the threshold voltage does not scale down with the same rate. This adds more demand on low-voltage analog building blocks. An increasing attention on floating gate circuits and systems has resulted in a number of interesting techniques and new floating gate circuits. This is expected to give creative analog designers another technique for circuit design. As a usable building block, floating gates are well established as non-volatile digital memory. Recent research has shown the feasibility of making analog memory-structures and with increased precision, post-fabrication circuit tuning is also possible.

Floating gate MOS transistors are widely used in digital word as EPROMs (Erasable programmable real only memories), EEPROMs (Electrically Erasable programmable real only memories), and flash memories. The primary principle is that the gate of a MOS transistor, embedded in SiO_2 (an insulator material), will maintain the stored charge for a long time. Floating gate devices were used in analog computation in a host of applications [80]. Low-voltage circuit building blocks such as: current mirrors, differential pairs, and OpAmps have been also reported in [81]. This aim of this work is

to initiate some new ideas of floating gate applications. It shows the feasibility of floating gate systems involved in real circuits with experimental verification.

A two-input floating gate transistor is shown in Fig. 6.1. The inputs are capacitively coupled to the floating gate (FG) and the transistor become with multiple control gates with a floating gate electrode. The voltage of the FG is determined as a linear sum of all input signals weighted by the capacitive coupling coefficients.

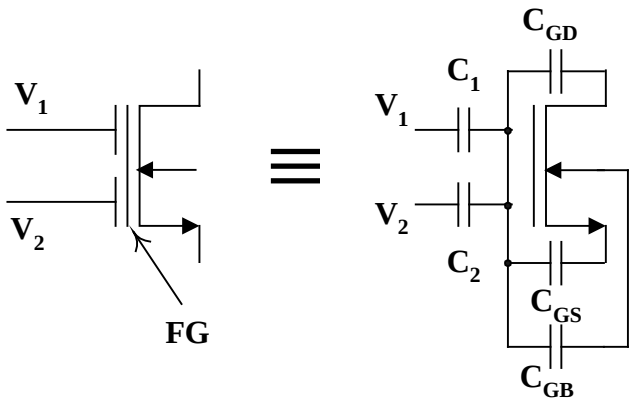

Fig. 6.1 Two-input floating gate transistor

Thus for the case of Fig. 6.1 and assuming that the initial floating charge at the FG is removed using ultraviolet light, we can write:

$$V_{FG} = \frac{C_{GB}}{C_{TOT}}V_B + \frac{C_{GD}}{C_{TOT}}V_D + \frac{C_{GS}}{C_{TOT}}V_S + \frac{C_1}{C_{TOT}}V_1 + \frac{C_2}{C_{TOT}}V_2 \qquad (6.1)$$

where C_{GB}, C_{GD}, C_{GS} is the capacitor formed between the FG and the substrate, the drain, and the source, respectively. V_B, V_D, V_S, is the potential of the substrate, the drain, and the source, respectively. $C_{TOT}=C_{GB}+C_{GD}+C_{GS}+C_1+C_2$. The control capacitances (C_1 and

C_2) are formed between the input gates (typically poly II layer) and the FG (usually poly I layer).

If a biasing dc voltage V_{bias} is applied at one gate and the signal V_{in} is applied to the other gate, the threshold voltage V_{Teq} seen from the signal gate is adjusted as shown in equation (6.2), assuming $C_1,C_2>>C_{GB},C_{GD},C_{GS}$. This can be utilized in low voltage applications. This programming property has been also used in circuit trimming and neural networks. Note also from equation (6.2) that there is an attenuation in the transconductance by the factor $(C_1+C_2)/C_2$ which can be used for linearization as discussed in section 2.1.1.2

$$\begin{aligned} I_D = \beta[V_{FG} - V_T]^2 &= \beta\left[\frac{C_1}{C_1+C_2}V_{bias} + \frac{C_2}{C_1+C_2}V_{in} - V_T\right]^2 \\ &= \beta\left(\frac{C_2}{C_1+C_2}\right)^2\left[V_{in} - \left(\frac{V_T - [C_1/(C_1+C_2)]V_{bias}}{[C_2/(C_1+C_2)]}\right)\right]^2 \\ &\Rightarrow V_{Teq} = \left(\frac{V_T - (C_1/C_{TOT})V_{bias}}{(C_2/C_{TOT})}\right) \end{aligned} \tag{6.2}$$

Equation (6.2) shows V_{Teq} can be less that V_T depending on the value of V_{bias}, C_1, C_2. The effective transconductance g_{meq} is given by:

$$g_{meq} = \frac{C_2}{C_1+C_2}g_{mFG} \tag{6.3a}$$

The effective output conductance g_{oeq} is given by:

$$g_{oeq} = g_{oFG} + \frac{C_{GD}}{C_{TOT}}g_{mFG} \cong g_{oFG}\ (for\ C_{GD} << C_{TOT}) \tag{6.3b}$$

Using a floating gate transistor, as shown in Fig. 6.1, as the input stage of an OpAmp, the equivalent gain A_{0eq}, the equivalent gain-bandwidth product GB_{eq}, and the equivalent SR_{eq} can be written, using equations (6.3a) and (6.3b), as :

$$A_{oeq} = \frac{g_{meq}}{g_{oeq}} \cong \frac{C_2}{C_1 + C_2} A_{oFG} \tag{6.4a}$$

$$GB_{eq} = \frac{g_{meq}}{C_L} = \frac{C_2}{C_1 + C_2} GB_{FG}$$, where C_L is the load capacitance (6.4b)

$$SR_{eq} = \frac{I_{bias}}{C_L} = SR_{FG} \tag{6.4c}$$

In measurement and instrumentation applications, accuracy limitation is determined by the A/D converter. In these applications, high resolution and moderate conversion rate are required. The important factors affecting the conversion accuracy, using a switched capacitor implementation, include charge injection, clock feedthrough, offset voltage, finite dc gain, finite GBW, limited slew rate, and input referred noise of the operational amplifier (OpAmp) used.

In order to operate under low voltage requirements, with high resolution, a fully differential two-stage OpAmp using floating gate technique has been designed [81]. High-resolution performance can be achieved even if the integrator does not settle to the full resolution of the converter, provided that the settling is linearly dependent on the input signal. The settling error can be nonlinear due to two possible reasons: saturation of the input stage or slew limitation of the output stage. For very high-resolution converters, the nonlinear settling can be a dominant factor in limiting the performance [82].

To avoid saturation limitations in the input stage, a large overdrive voltage V_{dsat} must be used for the input transistors, which cannot be afforded for low voltage design. Otherwise, the integrator needs to be designed to settle to the full resolution of the converter [83]. Another solution, to reduce saturation limitations, is attenuating the input voltage. This can be naturally implemented by using floating gate transistors at the input stage of the OpAmp. The floating gate technique also provides a mean to shift the input dc bias voltage for proper biasing of the input stage and optimization of the dynamic range.

The use of a fully differential structure enhances the power supply rejection, and reduces the effects of charge injection, clock feedthrough, and even harmonic distortion. A common-mode feedback (CMFB) circuit is implemented to fix the common-mode voltage of the OpAmp. It consists of a switched resistor common-mode detector and a continuous-time voltage comparator [84].

This chapter is organized as follows: Section 6.2 shows the incremental A/D converter architecture and operation. Design considerations of the OpAmp and the switches are discussed in section 6.3. Designs of different building blocks are introduced in section 6.4. The experimental results are shown in section 6.5. Finally, concluding remarks are drawn in section 6.6.

6.2. Incremental A/D Converter Architecture and Operation

The block diagram of the incremental A/D converter [85] is shown in Fig. 6.2(a). The switched capacitor realization of the incremental A/D converter is shown in Fig.

6.2(b). The structure contains an integrator and a latched comparator in a feedback loop similar to a conventional sigma delta converter. Each integration cycle is controlled by two-phase non-overlapping clocks φ_1 and φ_2. During φ_1, the input is sampled on capacitor C_1 and the latched comparator is strobed. During φ_2, either V_R or $-V_R$, depending on the sign of the output as determined by the comparator in the previous phase, is fed back to the integrator, and the charge stored on C_1 is transferred to C_2.

The operation of the converter can be seen as either adding $(C_1/C_2)(V_{id}-2V_R)$ or $(C_1/C_2)(V_{id}+2V_R)$ to the output voltage in each integration cycle. Thus effectively $(C_1/C_2)V_{id}$ is added to the output voltage in each integration cycle, while $2(C_1/C_2)V_R$ is added to the output voltage if V_{od} is negative, and subtracted if V_{od} is positive, as detected by the comparator.

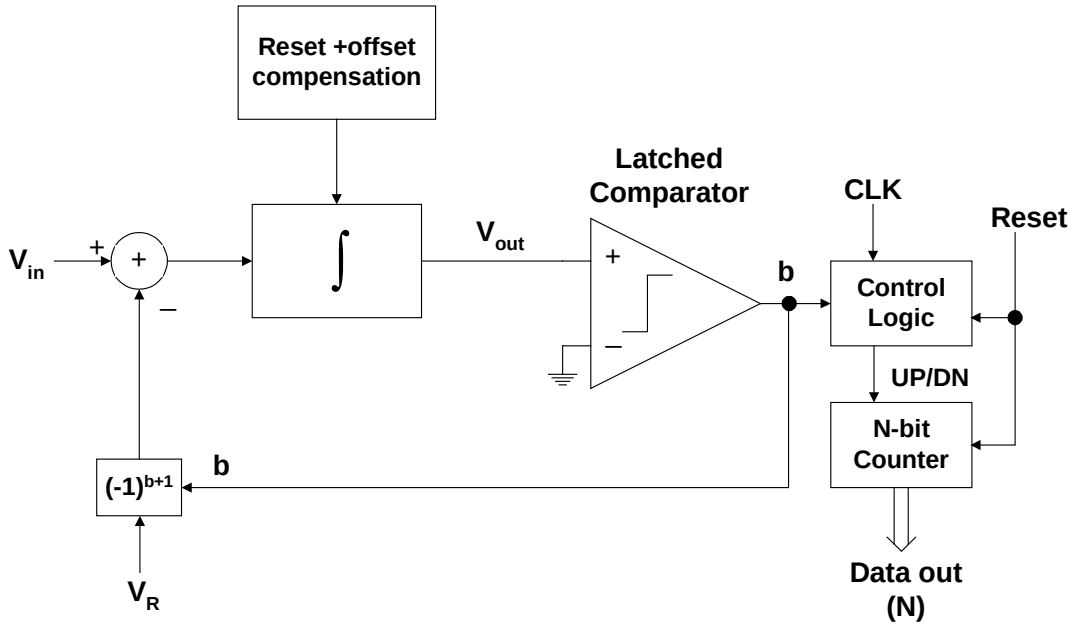

Fig. 6.2(a) Block diagram of incremental A/D converter

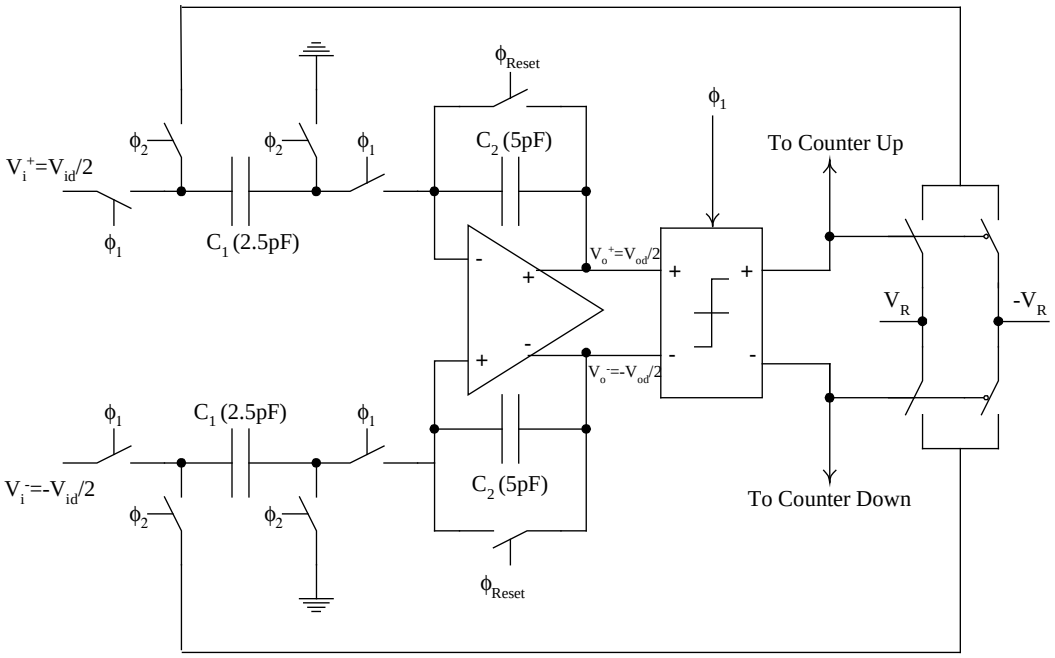

Fig. 6.2(b) Fully differential switched capacitor realization of the incremental A/D converter

So at the end of one conversion cycle (2^n integration cycles), the output voltage can be described by:

$$V_{od} = \frac{C_1}{C_2}\left[2^n V_{id} - 2(N_{up} - N_{down})V_R\right] \tag{6.5}$$

where N_{up} indicates the number of subtractions of $2V_R$, while $N_{down} = 2^n - N_{up}$ indicates the number of additions of $2V_R$. Using an Up/Down counter, the difference between N_{up} and N_{down} can be calculated, i.e., the content of the counter, at the end of each conversion cycle, will be:

$$N = N_{UP} - N_{DOWN} \tag{6.6}$$

At the beginning of each conversion cycle, the integrator and the counter are both reset. Then from equation (6.5) and since $|V_{out}| < 2(C_1/C_2)V_R$, we have:

$$N = 2^n \left(V_{id} / 2V_R \right) + \varepsilon \text{, where } |\varepsilon| < 2 \tag{6.7}$$

From equation (6.7) note that to achieve 15 bits of accuracy, with quantization error ≤ 1LSB, 2^{16} integration cycles are needed. The equivalent number of bits of accuracy (ENOB) can be increased if we increase n, where ENOB is calculated using the following formula:

$$ENOB = \log_2 \left| \frac{2^n}{N - (2^n V_{in} / V_{ref})} \right| \tag{6.8a}$$

$$ENOB = n - \log_2 \left| N - (2^n V_{in} / V_{ref}) \right| = n - \log_2 \varepsilon \tag{6.8b}$$

It is also affected by any accuracy error ε introduced by the non-idealities of different components in the circuit. The aim of this design is to minimize the accuracy error ε to be less than one least significant bit.

In order to compensate for offsets, a simple digital correction scheme can be used. This can be done, prior to the signal conversion phase, by grounding the converter inputs and storing the counter content in a latch after a complete initial calibration conversion cycle. The content of the counter corresponds to the input offset voltage. The digitally stored output referred offset can be subtracted digitally from the counter content after each signal conversion cycle. This offset correction scheme is effective in compensating for signal independent errors such as the input reffered offset of the OpAmp. The initial

calibration cycle can be also repeated from time to time to account for any possible time variations in the offset.

6.3. Design Considerations

In this section the specifications of different building blocks are determined. There are two basic building blocks in the system. The operational amplifier, the comparator and the additional switches and capacitors used for integration. It can be predicted that the performance of the overall system will be sensitive to the non-idealities of the operational amplifier. Those include finite dc gain, finite gain bandwidth product, finite slew rate, nonlinearities, dc offsets, and noise (including both thermal and flicker noises). The system is also sensitive to the noise produced in the sampling switches (thermal noise) simply because they are just at the input. On the other hand, the circuit imperfections and the noise of the comparator have a little impact on the overall performance of the modulator, because those effects will be attenuated by the large low-frequency gain of the first integrator.

The integrator output needs to settle completely in one time slot. The time slot allocated for the OpAmp to settle is less than half clock period to allow for non-ovelapping. The output of the integrator should settle to the desired ouput with a given accuracy within this time slot. Three main factors limit the settling of the OpAmp. First, the finite gain bandwidth product of the OpAmp. Second, the limited slew rate of the OpAmp. Third, the RC time constant of the MOS switches and the switched capacitors.

The settling error due to the previously mentioned effects is divided into two categories: linear and non-linear. Linear settling error is signal independent such as that caused due to finite gain bandwidth product of the OpAmp, while non-linear settling error is signal dependent such as that caused due to limited slew rate of the OpAmp.

6.3.1 Noise

The error due to noise is less than E_n (LSB) [85], where:

$$E_n = 2^{n/2}\left(3V_n / 2V_R\right) \tag{6.9}$$

V_n is the input referred noise voltage and is contributed by the two uncorrelated noise sources: sampling noise and OpAmp noise V_{nOpAmp}.

$$V_n^2 = \left(4KT / C_1\right) + V_{nOpAmp}^2 \tag{6.10}$$

For C_1=2.5pF, V_R=0.5V, V_{nOpAmp}=100μV, and n=16, the resulting error due to noise is 0.1 LSB.

6.3.2 Effect of Finite DC Gain

Due to the finite dc gain of the OpAmp, the integrator transfer function will deviate from ideal and can be expressed as:

$$V_{od}(k) = (1-\delta)V_{od}(k-1) + (C_1 / C_2)(1 - 1/A - \delta)V_{id}(k) \tag{6.11a}$$

where $\delta = C_1/(AC_2)$

The above equation shows that the error due to non-zero δ is accumulative, i.e., the gain error δ in the current output does not appear in the current input only but also in the

previous input. Hence, after 2^n cycles, the error will be $2^n \delta$. For this error to be less than one LSB:

$$2^n\left(\frac{C_1}{AC_2}\right)<1 \Rightarrow A>2^n\frac{C_1}{C_2} \tag{6.11b}$$

Choosing $(C_1/C_2)=0.5$, results in a maximum output voltage step of 0.5V on each branch and that can be accomodated within the used power supply voltage. Thus for n = 16, the dc gain can be determined to be more than 90dB.

Fig. 6.3 shows the simulated output of the integrator for ideal components (ideal switches and ideal operational amplifier) for a constant input differential signal of 0.4V, a refernce volatge of ±0.5V, and $C_2=2C_1$. Note that the output steps are either $0.5(V_{id}-2V_R)$or $0.5(V_{id}+2V_R)$ depending on the output of the comparator.

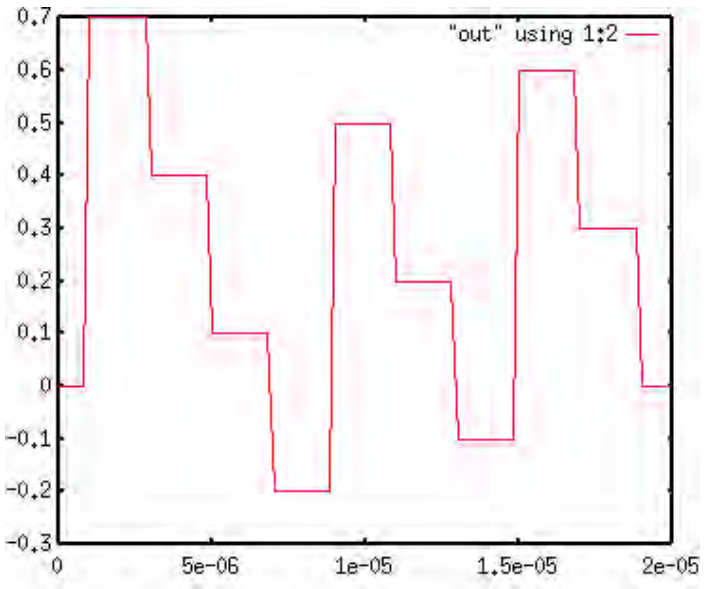

Fig. 6.3 Output of the integrator for ideal componenets for $V_{id}=0.4V$ and $V_R=0.5V$

Fig. 6.4 shows the effect of the finite OpAmp dc gain on the ENOB. This is calculated using the formula given in equation (6.8). It is shown that we need at leat 90dB of dc gain to achieve the 16 bits of accuracy which is consistent with equation (6.11b). It is worth mentioning that generally increasing the open loop dc gain of OpAmp helps reduce distortion due to the OpAmp non-linearities. It is also noticed that the required gain is large and can be reduced by using an integrator that has a low sensitivity for the finite dc gain. Assuming equal floating gate capacitors, and according to equation (6.4a), $A_{0eq}=0.5A_{0FG}$.

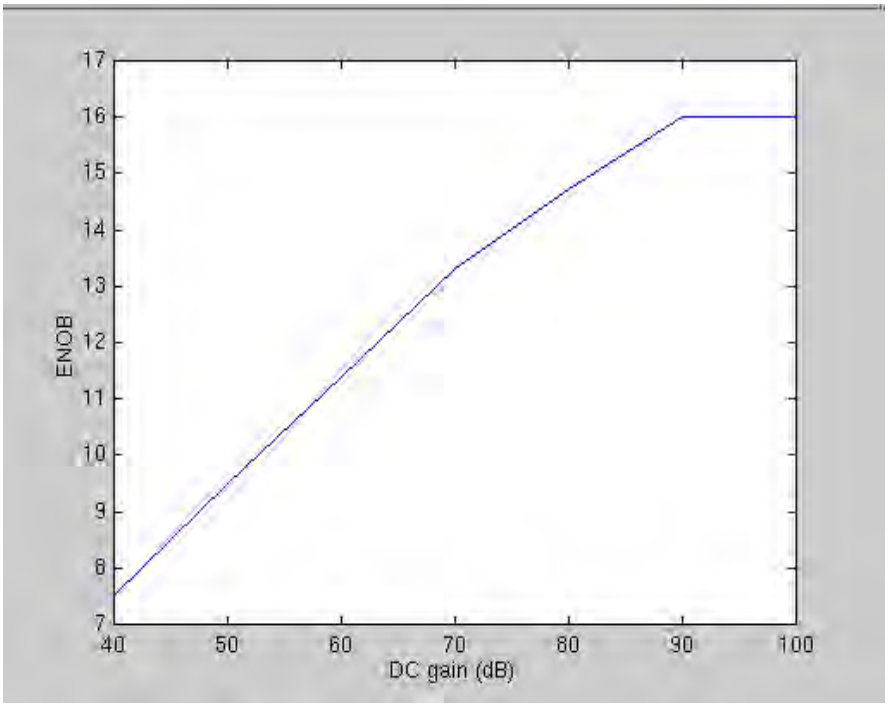

Fig. 6.4 Effect of the finite OpAmp dc gain on the ENOB

6.3.3 Effect of Finite GBW

Because of the finite GBW of the OpAmp, the output voltage will not settle to its final value during φ_2. If the OpAmp is bandwidth limited, the settling error will be $V_{in}e^{-t_{on}/\tau}\left(C_1/C_2\right)$, where t_{on} is the pulse duration of φ_2 (800ns) and τ is given by:

$$\tau = \frac{1}{GBW}\left(1+\frac{C_1+C_{inp}}{C_1+C_{M1}+C_{M2}}\right) \tag{6.12}$$

where C_{inp} is the amplifier input capacitance, C_{M1} and C_{M2} are the capacitances used in the common-mode detection circuit. Since the error is linearly dependent on the input voltage, it will not degrade the converter linearity. It will contribute only to a gain error $e^{-t_{on}/\tau}$. This means that the settling error does not have to be less than one LSB. For a settling error less than 0.1%, the time constant τ has to be less than $t_{on}/7$ corresponding to a GBW of 2.2MHz. Assuming equal floating gate capacitors, and according to equation (6.4b), $GB_{eq}=0.5GB_{FG}$.

6.3.4 Effect of Finite Switch Resistance

Finite switch resistance results in a settling error due to incomplete charging or discharging of the capacitor C_1. Since the switch resistance is a function of the input voltage, the settling error will be nonlinear and has to be less than one LSB.

$$e^{-t_{on}/(2R_{on}C_1)} < \frac{1}{2^{16}} \tag{6.13}$$

For C_1 = 2.5pF, the maximum switch resistance is 14.4kΩ. Transmission gate switches are used to ensure this condition is satisfied in the whole input voltage range.

For the used technology, V_{TN}=0.7V (around 0.9V including body effect), and K_N=116μA/V^2. The ON resistance can be calculated for the worst case of overdrive voltage, i.e., input signal at the middle. The value of the required 14.4kΩ corresponds to (W/L)=6 for an N-type transistor.

6.3.5 Effect of Finite Slew Rate

If the OpAmp is slew rate limited, the settling error will be a nonlinear function of the input signal. The worst case happens when the amplifier shifts by the maximum voltage step, which is 0.5V on each branch. The condition for the OpAmp to be bandwidth limited is:

$$SR > \frac{\Delta V_{\max}}{\tau} \Rightarrow SR > 9.4\frac{V}{\mu S} \tag{6.14}$$

According to equation (6.4c), the slew rate is the same with and without floating gates.

6.4. Block Design

6.4.1 Operational Amplifier (OpAmp)

A two-stage OpAmp is designed to be used in the SC integrator. Since the amplifier is driving only capacitive loads, no buffer stage is needed at the output. Fig. 6.5 shows the OpAmp circuit. Since PMOS transistors have less flicker noise than NMOS transistors, a p-type differential pair is used to reduce the input referred noise. However, due to the low voltage supply and large threshold voltage of PMOS transistors, the transistor V_{dsat} will be quite small. Hence, the input linear range is significantly small.

Although the OpAmp is used in a negative feedback configuration, which ensures that input voltage is virtual ground at steady state, a significant input voltage is applied to the OpAmp at the moment when φ_2 goes high. If this transient voltage is high enough, it may drive the input differential pair to the nonlinear region, which causes the settling error to be signal dependent.

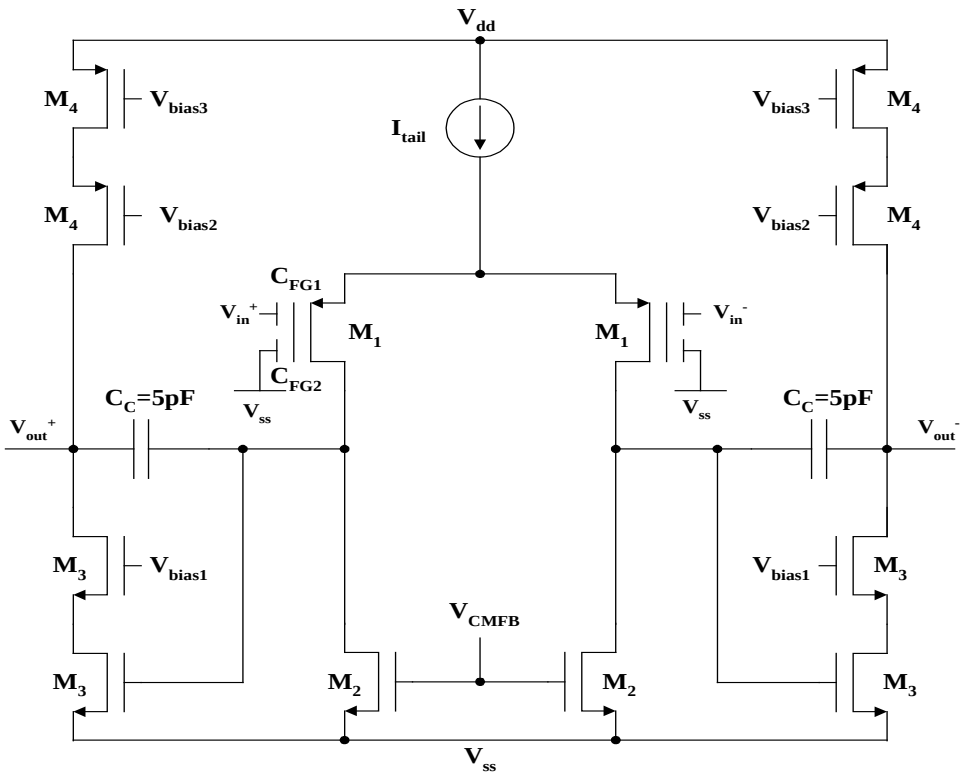

Fig. 6.5 Circuit implementation of the OpAmp

One way to avoid this problem is to attenuate input signal using floating gate (FG) differential pair as shown in Fig. 6.5. The voltage at the floating gate is given by:

$$V_{FG} = k_1 V_{in} + (1 - k_1) V_{ss} \tag{6.15}$$

If k_1=0.5, the common-mode FG voltage is –0.5V to make some room for signal swing. The input voltage is attenuated by a factor of 0.5.

The OpAmp design equations are as follows:

$$GBW = \frac{g_{meff}}{C_C} \tag{6.16}$$

$$PM = 90 - \tan^{-1}\left(\frac{g_{meff}}{g_{m3}}\frac{C_L}{C_C}\right) - \tan^{-1}\left(\frac{g_{meff}}{g_{m3}}\right) \tag{6.17}$$

$$\text{where } g_{meff} = \frac{C_{FG1}}{C_{FG1} + C_{FG2}} g_{m1}$$

$$V_{nOpAmp}^2 = \frac{2}{K_1^2}\left(V_{n1}^2 + \left(\frac{g_{m2}}{g_{meff}}\right)^2 V_{n2}^2\right), \text{ where } k_1 = \frac{C_{FG1}}{C_{FG1} + C_{FG2}} \tag{6.18}$$

The frequency response of the OpAmp is shown in Fig. 6.6. The total input referred noise is dominated by flicker noise of the NMOS transistor M2. Fig. 6.7 shows the positive and negative slew rates of the OpAmp, which are about 9.7V/μS and 9.8V/μS respectively. Table 6.1 summarizes the specifications of the OpAmp.

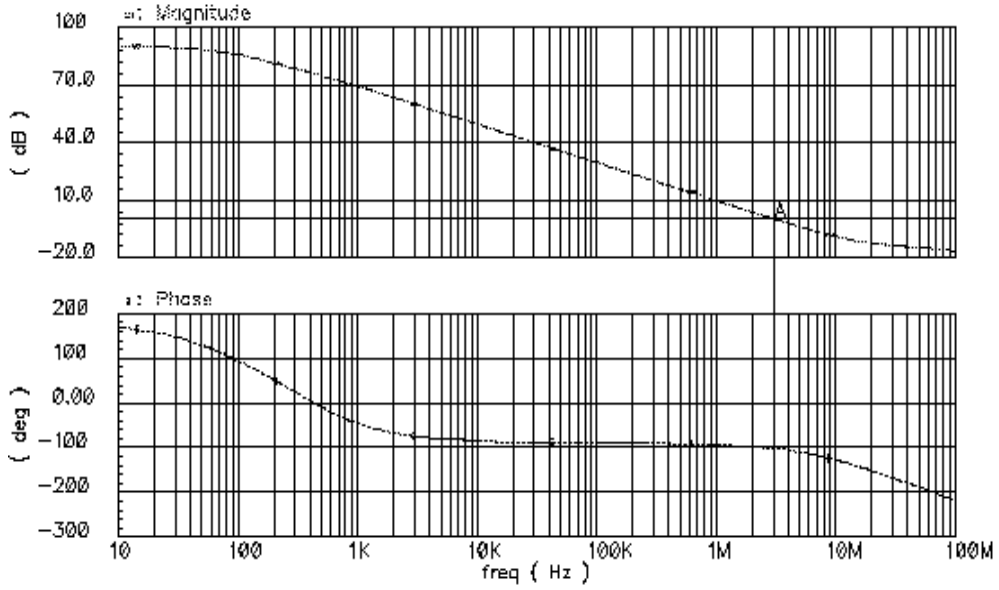

Fig. 6.6 Frequency response of the OpAmp

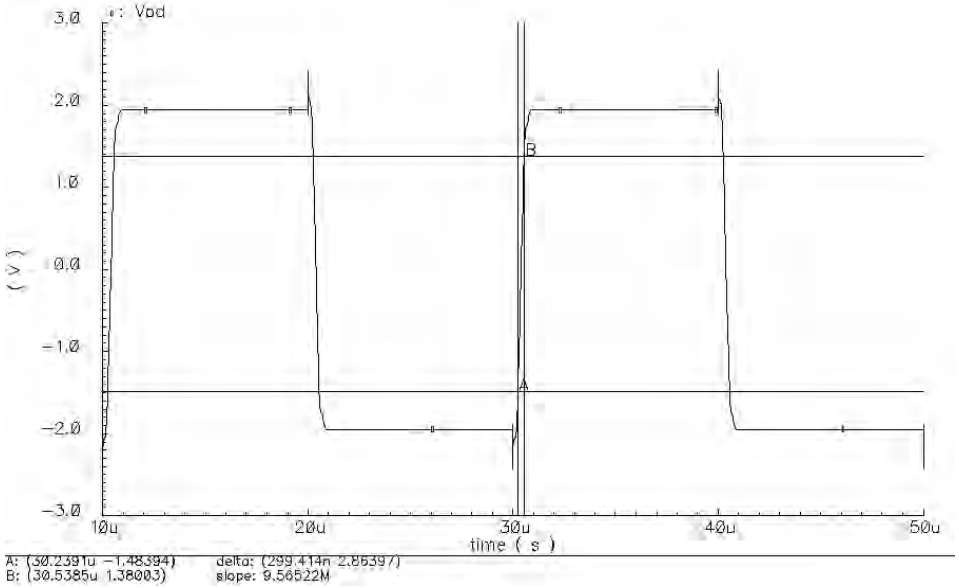

Fig. 6.7 Transient response of the OpAmp

Table 6.1 Specifications of the OpAmp

Parameter	**Required**	**Value**
DC gain	> 90 dB	91 dB
GBW	> 2.2 MHZ	3 MHz
Slew rate	> 9.4 V/μS	9.7 V/μS
I_{tail}	minimum	70 μA
V_{noise}	≤ 100 μV	100 μV

6.4.2 Comparator

The performance of the sigma delta converter is relatively insensitive to the comparator offset as it is divided by the integrator gain when referred to the input. The comparator used is based on the regenerative latch shown in Fig. 6.8.

The cross-coupled devices, M3, M4, M7, and M8 are strobed at their drains rather than their sources to eliminate the backgating effect and promote faster regeneration. The latch is strobed at the beginning of the sampling phase when φ_1 transitions from low to high. The latch is reset after the falling edge of φ_1 by switching on the PMOS transistors M_9 and M_{10}.

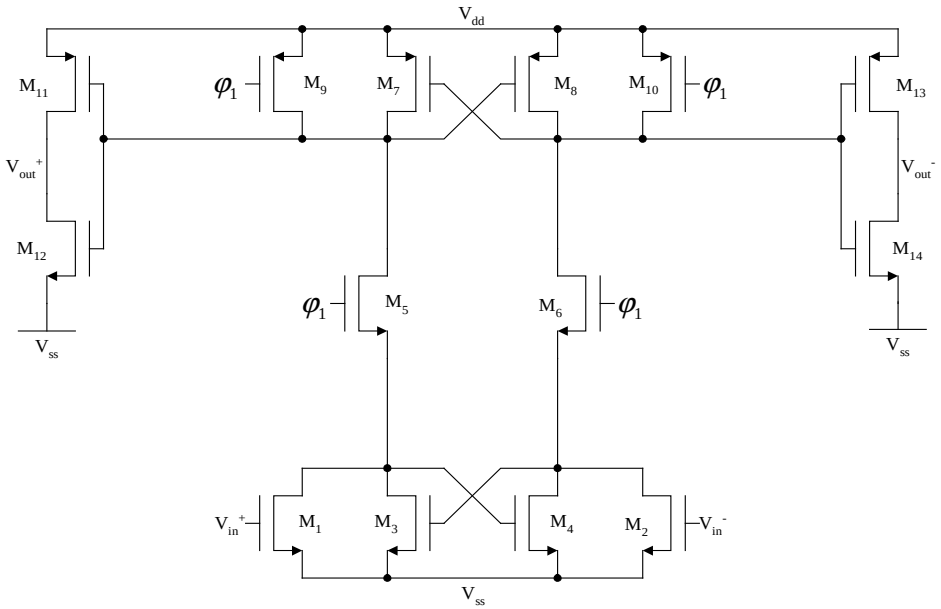

Fig. 6.8 Circuit implementation of the comparator

6.4.3 CMFB Circuit

As the case for any fully differential structure, we need an extra circuit to control the dc common-mode voltage at different nodes and to reject common-mode signals. This is performed by means of a common-mode feedback loop. This of course will increase the complexity of the design and has to be designed carefully.

The common-mode feedback circuit used combines both switched capacitor and continuous time techniques. The common-mode detection was implemented using two switched resistors as shown in Fig. 6.9, while the comparison of the common-mode voltage with the required reference voltage (zero in our case) is done using a continuous time comparator.

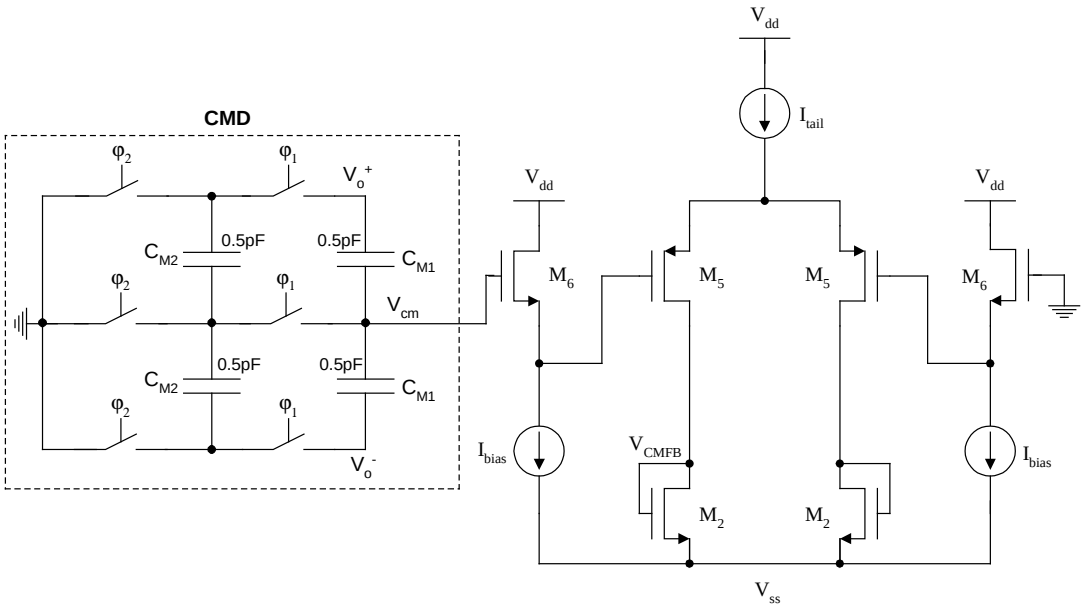

Fig. 6.9 CMFB circuit implementation

The switched-capcaitor common-mode detector (CMD) circuit is used to detect the common-mode output voltage of the OpAmp. The response of this circuit is expressed as

$$V_{cm} = \frac{0.5}{1 + \frac{C_{M1}}{C_{M2}} - \frac{C_{M1}}{C_{M2}} Z^{-1}} \left(V_o^+ + V_o^- \right) \tag{6.19}$$

This is a low pass response. The output of this CMD circuit is compared with ground (0V). The output of the comparator, V_{CMFB} is used to correct the common-mode voltage of the OpAmp. Level shift transistors M_6 are used to bias the p-type differential pair M_5 properly.

A simple design procedure for the incremental A/D converter, given a required accuracy, i.e., an effective number of bits , can be summarized as follows:

1. Calculate the value of the capacitor C_1 for 0.1LSB error as given by equations (6.9) and (6.10).
2. Choose the value of the capacitor C_2 for a reasonable OpAmp output voltage swing that complies with the supply voltage.
3. The ON resistance of the switches is calculated for a 1LSB settling error according to equation (6.13).
4. The required value of the DC gain of the OpAmp is chosen according to Fig. 6.4 for a 1LSB error.
5. The required value of the GBW of the OpAmp is chosen according to equation (6.12) for 0.1% settling error.
6. The required value of the SR of the OpAmp is chosen such that the OpAmp is bandwidth limited according to equation (6.14) to avoid nonlinear settling.

6.5. Measurement Results

The converter has been implemented in 0.5μm CMOS technology with V_{TN}=0.65V and V_{TP}=-0.90V. The chip prototype occupies an area of 0.2mm^2. The chip micrograph is shown in Fig. 6.10.

The circuit has been tested using the data acquisition cards of National Instruments while operating from a power supply voltage of ±1V. The test setup is shown in Fig. 6.11. The 6071E multifunction I/O card, which has 12 bits of resolution, is used to generate the differential analog inputs. The 6533 digital I/O card is used to acquire the

digital output of the comparator that is then processed to obtain the equivalent number of counts N.

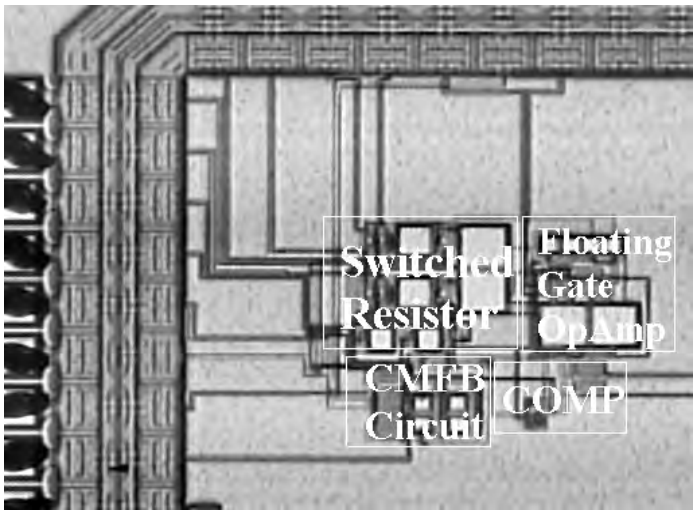

Fig. 6.10 Chip micrograph

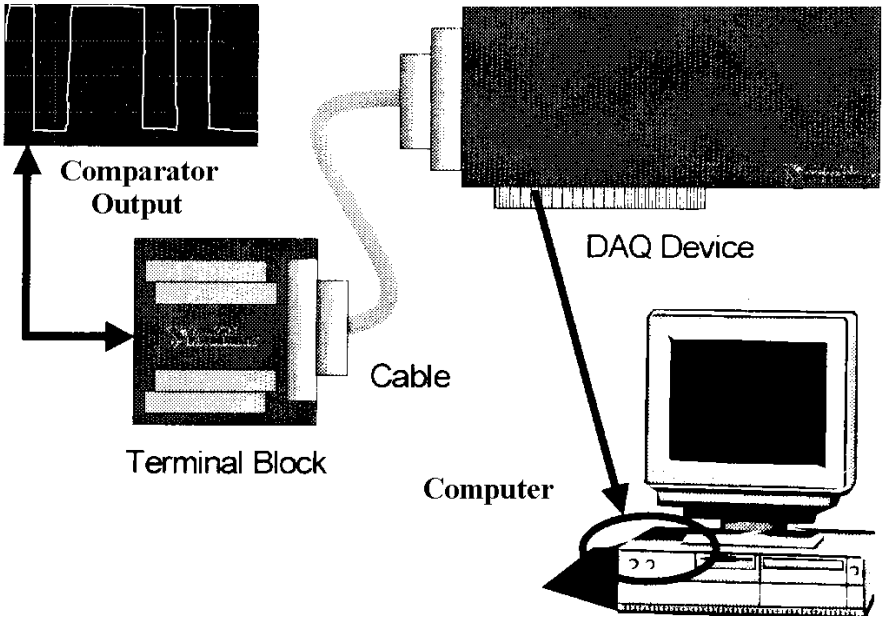

Fig. 6.11 Measurement setup

Fig. 6.12 shows the measured INL for 11 bits of resolution. The maximum integral nonlinearity (INL) is ±0.9LSB. The measured raw offset is 35mV, which can be compensated as discussed in section 6.2. The converter operates at a clock frequency of 500kHz and consumes less than 1mW. The converter has been designed for 15 bits of accuracy. Due to the limited accuracy of the measurement equipment, we were able to measure 11 bits of resolution.

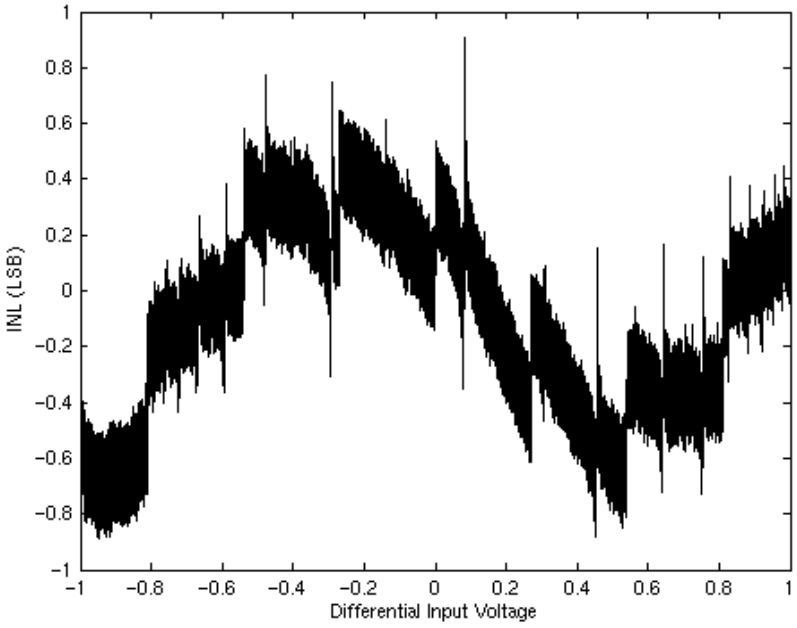

Fig. 6.12 Measured integral nonlinearity

6.6. Conclusions

The implementation of an incremental A/D converter for a power supply voltage of ±1V has been presented. The design relies on using floating gate technique in order to

reduce the effect of nonlinear settling due to possible saturation of the input stage and to achieve good performance under low voltage operation

Different design considerations for low voltage operation and high accuracy performance have been discussed. The block design of different building blocks, including the operational amplifier, the CMFB circuit, and the comparator has been shown.

The A/D converter operates at a clock frequency of 500kHz and consumes 0.95mW (including biasing and CMFB circuitry). The chip prototype occupies an area of $0.2mm^2$.

The converter has been designed for 15 bits of accuracy. Due to the limited accuracy of the measurement equipment (the analog input generation accuracy), we were able to measure 11 bits of resolution with a maximum INL of ±0.9LSB.

CHAPTER VII

CONCLUSIONS

In this dissertation, the design issues of high frequency continuous-time integrated filters have been examined. What mainly limit the performance of an analog filter are the non-idealities of the used building blocks and the circuit architecture. Several novel techniques and architectures have been proposed. On the circuit level, new building blocks have been introduced. A new pseudo differential fully balanced fully symmetric OTA structure has been shown. An economical CMFB strategy, with the appropriate arrangement of cascaded pseudo differential OTAs in a filter, has been shown.

A new dual-mode OTA structure was introduced. The OTA has been used to implement a low pass filter used as a channel select filter in a direct conversion dual-mode receiver for both Bluetooth and IEEE 802.11b (WLAN). Different design trade-offs have been investigated. A digital automatic tuning scheme was proposed.

Some novel circuit architectures have been also presented. A new 4^{th} order bandpass tunable LC filter structure has been shown. The proposed structure has the unique feature of emulating the magnetic coupling between the inductors. This provides bandwidth tuning while maintaining small passband ripple when compared with previously published filters using on-chip transformers.

A novel approach for implementing ROM-less DDFS has been presented. This approach is based on piecewise linear approximation of the sine function. The proposed

architecture is shown to have significant area and power savings at high clock rates compared to the recently reported structures in the literature. This renders the proposed structure more suitable for low power portable applications.

REFERENCES

[1] K.W.H. Ng, V.S.L. Cheung, and H. Luong, "A 3-V 44-MHz switched-capacitor bandpass filter for digital video application," in *Proc. of the IEEE International Symposium on Circuits and Systems*, Arizona, May 2002, pp. IV.627-IV.630.

[2] S. Kiriaki, T. Lakshmi Viswanathan, G. Feygin, B. Staszewski, R. Person, B. Krenik, M. de Wit, and K. Nagaraj, "A 160-MHz analog equalizer for magnetic disk read channels," *IEEE J. Solid-State Circuits*, vol. 32, no. 11, pp. 1839-1850, November 1997.

[3] K. Yido, H. Hyungki, C. Yongsik, L. Jeongwoo, P. Joonbae, L. Kyeongho Lee, J. Deog-Kyoon, and K. Wonchan, "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 536-542, May 2002.

[4] G. Chunbing, L. Chi-Wa; C. Yu-Wing, I. Hsu, T. Kan, D. Leung, A. Chan, and H.C. Luong, "A fully integrated 900-MHz CMOS wireless receiver with on-chip RF and IF filters and 79-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1084-1089, August 2002.

[5] K. Hettak, C.J. Verver, and M.G. Stubbs, "Overlapping, multiple CPW stub structures for high density MMICs," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 311-314, May, 2001.

[6] C.C.W. Ruppel, L. Reindl, and R. Weigel, "SAW devices and their wireless communications applications," *IEEE Microwave Magazine*, vol. 3, no.2, pp. 65-71, June 2002.

[7] J.H.Visser, M.J. Vellekoop, A.Venema, E. van der Drift, P.J.M. Rek, A.J. Nederlof, and M.S. Nieuwenhuizen, "Surface acoustic wave filters in ZnO-SiO_2-Si layered structures," in *Proc. of the Ultrasonics Symposium*, Montreal, Canada, 1989, vol. 1, pp. 195-200.

[8] J. Machui, G. Mullerm, W. Ruile, L. Reindl, R. Weigel, and P. Russer, "A new low loss filter structure with extremely wide bandwidth for mobile communication systems," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1501-1504, June, 1993.

[9] T.Deliyannis, Y. Sun, and J.K. Fildler, Continuous-Time Active Filter Design, CRC Press, Boca Raton, 1999.

[10] R.P. Sallen and E.L. Key, "A practical method of designing RC-active filters," *IEEE Trans. Circuit Theory*, vol. CT-2, pp. 74-85, March 1955.

[11] W.V. Kenzle, "FIESTA-II a software tool for electronic filter design," M.S. thesis, Texas A&M University, College Station, 1997.

[12] W.M. Snelgrove and A.S. Sedra "Optimization of dynamic range in cascade active filters," *in Proc. IEEE Symp. Circuits & Systems*, Philadelphia, PA, 1978, pp. 151-155.

[13] K.R. Laker, R. Schaumann, and M.S. Ghausi, "Multiple-loop feedback topologies for the design of low-sensitivity active filters," *IEEE Trans. Circuits & Systems*, vol. 26, pp. 1-21, January 1979.

[14] P.O. Brackett, and A.S. Sedra, "Direct SFG simulation of LC ladder networks with applications to active filter design," *IEEE Trans. Circuit & Systems*, vol. 23, pp. 61-67, February 1976.

[15] G. Hurtig, "The primary resonator block technique of filter synthesis," in *Proc. Int. Filter Symp.*, 1972, pp. 84-85.

[16] C. Acar and M.S. Ghausi "Design of high-order active filters in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 13, no. 2, pp. 273-276, April 1978.

[17] K. Martin and A.S. Sedra, "Design of signal-flow graph (SFG) active filters," *IEEE Trans. Circuit & Sytems*, vol. 25, pp. 185-195, April 1978.

[18] J. Silva-Martínez, M.S.J. Steyaert, and W. Sansen, "A 10.7MHz 68dB CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1843-1853, December 1992.

[19] H. Khorramabadi and P.R. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939-948, December 1984.

[20] D. Li and Y. Tsividis, "A 1.9GHz Si active LC filter with on-chip automatic tuning," *in International Solid-State Circuits Conference*, San Francisco, California, 2001, pp. 368-369.

[21] J.M. Stevenson and E. Sánchez-Sinencio, "An accurate quality factor tuning scheme for IF and high-Q continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1970-1978, December 1998.

[22] H. Huang and E.K.F. Lee, "Digital frequency and Q tuning technique for low-voltage active filters," *Electronic Letters*, vol. 35, no.8, pp. 635-636, April 1999.

[23] W. Dehaene, M.S.J. Steyaert, and W. Sansen, "A 50 MHz standard CMOS pulse equalizer for hard disk read channels," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 977-988, July 1997.

[24] N. Rao, V. Balan, and R. Contreras, "A 3V 10-100 MHz continuous time seventh order 0.05^0 equiripple linear phase filter," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1676-1682, November 1999.

[25] N. Rao, V. Balan, R. Contreras, J-G. Chern, and Y. Wang, "A 150 MHz continuous time seventh order 0.05^0 equiripple linear phase filter," *in Proc. of the IEEE International Symposium on Circuits and Systems*, Orlando, Florida, 1999, vol. 2, pp. 664-666.

[26] C. Wu and S. Hsiao, "The design of a 3-V 900-MHz CMOS bandpass amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 159-168, February 1997.

[27] K. Chan, M. Do, K. Yeo, and J. Ma, "1.5 V 1.8 GHz bandpass amplifier," *in Proc. of the IEE Circuits Devices Systems*, December 2000, vol. 147, no. 6, pp. 331-333.

[28] L. Fanucci, G. D'Angelo, A. Monterastelli, M. Paparo, and B. Neri, "Fully integrated low-noise-amplifier with high quality factor L-C filter for 1.8 GHz wireless applications," *in the IEEE Symposium on Circuits and Systems*, Sydney, Australia, May 2001, vol. 4, pp. 462-465.

[29] J.A. Macedo and M.A. Copeland, "A 1.9 GHz silicon receiver with monolithic image filtering," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 378-386, March 1998.

[30] F. Svelto, G. Montagna, S. Deantoni, G. Braschi, and R. Castello, "Solutions for image rejection CMOS LNA", *in the IEEE Symposium on Circuits and Systems*, Geneva, Switzerland, May 2000, vol. 3, pp. 49-52.

[31] H. Samavati, H.R. Rategh, and T.H. Lee, "A 5-GHz wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765-772, May 2000.

[32] W.B. Kuhn, N.K. Yanduru, and A.S. Wyszynski, "Q-enhanced LC bandpass filters for integrated wireless applications," *IEEE Trans. Microwave Theory & Techniques*, vol. 46, no. 12, pp. 2577-2586, December 1998.

[33] T. Itakura, T. Ueno, H. Tanimoto, and T. Arai, "A 2 $V_{p\text{-}p}$ linear input range fully balanced CMOS transconductor and its application to a 2.5V 2.5MHz G_m-C LPF," *in Proc. of the IEEE Custom Integrated Circuits*, San Diego, California, 1999, pp. 509-512.

[34] A.Wyszynski and R.Schaumann, "Avoiding common mode feedback in continuous-time Gm-C filters by use of lossy integrators," *in the IEEE International Symp. on Circuits and Systems*, London, UK, 1994, vol. 5, pp. 281-284.

[35] Ahmed N. Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A low-voltage fully balanced OTA with common mode feedforward and inherent common mode feedback detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 663-668, April 2003.

[36] Ahmed N. Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A low-voltage fully balanced OTA with common mode feedforward and inherent common mode feedback detector," *in the European Solid-State Circuits Conference*, Florence, Italy, September 2002, pp. 191-194.

[37] Ahmed N. Mohieldin, Edgar Sánchez-Sinencio, and José Silva-Martínez, "Nonlinear Effects in Pseudo-differential OTAs with CMFB," *submitted May 2003 to the IEEE Transactions on Circuits and Systems.*

[38] J. Silva-Martínez, M.S.J. Steyaert, and W. Sansen, "A large-signal very low distortion for high-frequency continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 946-955, July 1991.

[39] J. Ramírez-Angulo, R.G. Carvajal, J. Tombs, and A. Torralba, "Low-voltage CMOS OpAmp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating gate transistors," *IEEE Trans. on Circuits and Systems-II*, vol. 48, no. 1, pp. 111-116, January 2001.

[40] P.W. Allen, B.J. Blalock, and G.A. Rincon, "A 1 V CMOS op amp using bulk-driven MOSFETs," *in the IEEE International Solid-State Circuits Conference*, San Francisco, California, February 1995, pp. 192-193.

[41] J.F. Duque-Carrillo, "Continuous-time common-mode feedback networks for fully-differential amplifiers: A comparative study," *in the IEEE International Symposium on Circuits and Systems*, Chicago, IL, May 1993, vol.2, pp. 1267-1270.

[42] J.F. Duque-Carrillo, "Control of common-mode component in CMOS continuous-time fully differential signal processing," *Analog Integrated Circuits and Signal Processing, An International Journal, Kluwer Academic Publishers*, vol.4, pp. 131-140, September 1993.

[43] W. M. Snelgrove and A. Shoval, "A balanced 0.9 μm CMOS transconductance-C filter tunable over the VHF range," *IEEE J. Solid-State Circuits*, vol. 27, no. 30, pp. 314-323, March 1992.

[44] F. Rezzi, A. Baschirotto, and R. Castello, "A 3V 12-55 MHz BiCMOS pseudo differential continuous-time filter," *IEEE Trans. on Circuits and Systems-I*, vol. 42, no. 11, pp. 896-903, November 1995.

[45] P. Kallam, E. Sánchez-Sinencio, and Aydin Ilker Karsilayan, "An enhanced adaptive q-tuning scheme for a 100-MHz fully symmetric OTA-based bandpass filter, " *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 585-593, April 2003.

[46] Z. Czarnul, T. Itakura, N. Dobashi, T. Ueno, T. Iida, and H. Tanimoto, "Design of fully balanced analog systems based on ordinary and/or modified single-ended opamps," *IEICE Trans. Fundamentals*, vol. E82-A, no. 2, pp. 256-270, February 1999.

[47] T. Itakura, T. Ueno, H. Tanimoto, A. Yasuda, R. Fujimoto, T. Arai, and H. Kokatsu "A 2.7-V 200-kHz, 49-dBm, stopband-IIP3, low-noise, fully balanced G_m-C filter IC," *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1155-1159, August 1999.

[48] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997.

[49] P.R. Gray, R.G. Meyer, *Analog Integrated Circuits. 3rd edition*, John Wiley & Sons, New York, 1993.

[50] E. Sánchez-Sinencio and J. Silva-Martínez, "CMOS transconductance amplifiers and active filters: A tutorial," *in the IEE Proc. Circuits Devices Systems* , February 2000, vol. 147, no. 1, pp. 3-12.

[51] Bluetooth Specification Version 1.0, http://www.bluetooth.com/specifications.asp, (accessed on 05/01/2003).

[52] IEEE 802® Standards, http://standards.ieee.org/getieee802/, (accessed on 05/01/2003).

[53] S. Lindfors, J. Jussila, K. Halonen, and L. Siren, "A 3-V continuous-time filter with on-chip tuning for IS-95," *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1150-1154, August 1999.

[54] T. Hollman, S. Lindfors, M. Lansirinne, J. Jussila, and K. Halonen, "A 2.7V CMOS dual-mode baseband filter for PDC and WCDMA," *in the European Solid-State Circuits Conference*, Stockholm, Sweden, September 2000.

[55] J. Jussila, A. Parssinen, and K. Halonen, "A channel selection filter for a WCDMA direct conversion receiver," *in the European Solid-State Circuits Conference*, Stockholm, Sweden, September 2000.

[56] H.A. Alzaher, H.O. Elwan, and M. Ismail, "A CMOS highly linear channel-select filter for 3G multistandard wireless receivers," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 27-37, January 2002.

[57] A. Yoshizawa, and Y.P. Tsividis, "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 357-364, March 2002.

[58] S. Pipilos, Y. P. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8GHz RLC filter with tunable center frequency and quality factor," *IEEE J. Solid-State Circuits*, vol. 31, no. 10, pp. 1517-1525, October 1996.

[59] R. Duncan, K. W. Martin, and A. Sedra, "A Q-enhanced active RLC bandpass filter," *IEEE Trans. on Circuits and Systems-II*, vol. 44, no. 5, pp. 341-346, May 1997.

[60] W. B. Kuhn, F. W. Stephenson, and A. Elshabini-Riad, "A 200MHz CMOS Q-enhanced LC bandpass filter," *IEEE J. IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1112-1122, August 1996.

[61] T. Soorapanth, and S.S. Wong, "A 0-dB IL 2140±30MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 579-586, May 2002.

[62] F. Dülger, E. Sánchez-Sinencio, and J. Silva-Martínez, "A 1.3V, 5mW, fully-integrated programmable bandpass filter at 2.1GHz in 0.35μm CMOS," *in the IEEE Custom Integrated Circuits Conference*, Orlando, Florida, 2002, pp. 283-286.

[63] A.M.Niknejad, R.G.Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, October 1998.

[64] A. I. Zverev, *Handbook of Filter Synthesis*, Wiley, New York, 1967.

[65] P. Wambacq, and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Kluwer Academic Publishers, Boston, 1998.

[66] A.T. Behr, M.C. Schneider, S. N. Filho, and C. G. Montoro, "Harmonic distortion caused by capacitors implemented with MOSFET gates," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, pp. 1470-1475, October 1992.

[67] A. N. Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martínez, "A 2.7V, 1.8GHz, 4th order tunable LC bandpass filter with ±0.25dB passband ripple," *in the European Solid-State Circuits Conference*, Florence, Italy, September 2002, pp. 343-346.

[68] A. N. Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martínez, "A 2.7V, 1.8GHz, 4th order tunable LC bandpass filter based on emulation of magnetically-coupled resonators," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, July 2003.

[69] A.M. Niknejad, "Modeling of passive elements with ASITIC," *IEEE Symposium of Radio Frequency Integrated Circuits*, Seattle, WA, 2002, pp. 303-306.

[70] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, Boston, 1998.

[71] D.A. Sunderland, R.A. Strauch, S.S. Wharfield, H.T. Peterson, and C.R. Cole "CMOS/SOS frequency synthesizer LSI circuit for spread spectrum communications," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 497-505, August. 1984.

[72] H.T. Nicholas III, H. Samueli, and B. Kim "The optimization of direct digital frequency synthesizer performance in the presence of finite wordlength effects," *in Proc. of the 42nd Annual Frequency Control Symp*., Baltimore, MD, 1988, pp. 357-363.

[73] A.M. Sodagar and G. R. Lahiji, "Mapping from phase to sine-amplitude in direct digital frequency synthesizers using parabolic approximation," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 12, pp. 1452-1457, December 2000.

[74] A. Bellaouar, M.S. O'brecht, A.M. Fahim, M.I. Elmasry "Low-power direct digital frequency synthesis for wireless communications," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 385-390, March 2000.

[75] S. Mortezapour, E.K F. Lee "Design of low-power ROM-less direct digital frequency synthesizer using nonlinear digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol.34, no.10, pp. 1350-1359, October 1999.

[76] J. Jiang and E.K.F. Lee "A ROM-less direct digital frequency synthesizer using segmented nonlinear digital-to-analog converter," *in the IEEE Custom Integrated Circuits Conf*., San Diego, California, 2001, pp.165-168.

[77] Ahmed N. Mohieldin, Ahmed Emira, and Edgar Sánchez-Sinencio, "A 100MHz, 8mW ROM-less quadrature direct digital frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1235-1243, October 2002.

[78] C. Meenakarn, and A. Thanachayanont, "100-MHZ CMOS direct digital synthesizer with 10-bit DAC," *in Proc. of the Asia-Pacific Conference on Circuits and Systems*, Bangkok, Thailand, 2002, pp. 385-388.

[79] B. Provost, and E. Sánchez-Sinencio, "On-chip ramp generators for mixed-signal BIST and ADC self-test, *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 263-273, February 2003.

[80] T. Shibata, and T. Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operations," *IEEE Trans. Electron Devices*, vol. 39, pp. 1444-1455, 1992.

[81] J. Ramírez-Angulo, S.C. Choi, and G. González-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circuits and Systems*, vol. 42, no. 11, pp. 971-974, November 1995.

[82] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti, "Modeling sigma-delta modulator non-idealities in Simulink," *in Proc. of the IEEE International Symposium on Circuits and Systems*, Orlando, Florida, 1999, vol. 2, pp. 384-387.

[83] Shahriar Rabii, and Bruce A. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June 1997.

[84] Ahmed N. Mohieldin, Ahmed Emira, and Edgar Sánchez-Sinencio, "A 2V 11Bit incremental A/D converter using floating gate technique," *in Proc. of the IEEE International Symposium on Circuits and Systems*, Scottsdale, Arizona, May 2002, pp. IV.667-IV-670.

[85] J. Robert, G.C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low-voltage CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 22, no. 2, pp. 157-163, April 1987.

[86] B. Razavi, *RF Microelectronics*, Prentice Hall Inc., New Jersey, 1998.

Appendix A

RF METRICS

1. Distortion

Consider a nonlinear system described by the following equation:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{A.1}$$

where y(t) and x(t) is the ouput and input of the system respectively.

Assume $x(t) = A\cos(\omega t)$, then from equation (A.1) we get:

$$y(t) = \alpha_0 + \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t) \tag{A.2a}$$

$$y(t) = \left(\alpha_0 + \frac{\alpha_2 A^2}{2}\right) + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \left(\frac{\alpha_2 A^2}{2}\right)\cos(2\omega t) + \left(\frac{\alpha_3 A^3}{4}\right)\cos(3\omega t) \tag{A.2b}$$

In equation (A.2b), the term with the input frequency is called the fundamental and the higher order terms the harmonics. Harmonic distortion factors (HD_i) provide a measure for the dostortion introduced by each harmonic for a given input signal level (using a single tone at a given frequency). HD_i is defined as the ratio of the output signal level of the i^{th} harmonic to that of the fundamental. The THD is the geometric mean of the distortion factors. The second harmonic distortion HD_2, the third harmonic distortion HD_3, and the total harmonic distortion THD are defined as (assuming $\alpha_1 A >> 3\alpha_3 A^3/4$):

$$HD_2 = \frac{\alpha_2 A}{2\alpha_1} \tag{A.3a}$$

$$HD_3 = \frac{\alpha_3 A^2}{4\alpha_1} \tag{A.3b}$$

$$THD = \sqrt{HD_2^2 + HD_3^2 + HD_4^2 + ...} \tag{A.3c}$$

For fully differential systems, even harmonics will vanish and only odd harmonics remain. In reality, however, mismatches corrupt the symmetry, yielding finite even order harmonics. In a fully differential system with ε% mismatch and from equation (A.3a), HD_2 is given by:

$$HD_2 = \varepsilon \frac{\alpha_2 A}{2\alpha_1} \tag{A.4}$$

1-dB compression point

The 1-dB compression point is defined as the point where the fundamental gain deviates from the ideal small signal gain by 1 dB, as shown in Fig. A.1. From the previous definition and from equation (A.2b), we have:

$$20\log\left(\alpha_1 A_{1-dB} + \frac{3\alpha_3 A_{1-dB}^3}{4}\right) = 20\log(\alpha_1 A_{1-dB}) - 1 = 20\log(0.89125\alpha_1 A_{1-dB}) \tag{A.5}$$

$$A_{1-dB}^2 = 0.10875\frac{4}{3}\frac{|\alpha_1|}{|\alpha_3|} = k\frac{|\alpha_1|}{|\alpha_3|} \text{ , where k=0.145} \tag{A.6}$$

Thus at the 1-dB compression point, the value of HD_3 can be calculated as:

$$HD_3 = \frac{1}{4}\frac{k}{A_{1-dB}}A^2 = \frac{0.145}{4}\frac{|\alpha_3|}{|\alpha_1|}\frac{|\alpha_1|}{|\alpha_3|} = \frac{0.145}{4}\times 100\% = 3.6\% \tag{A.7}$$

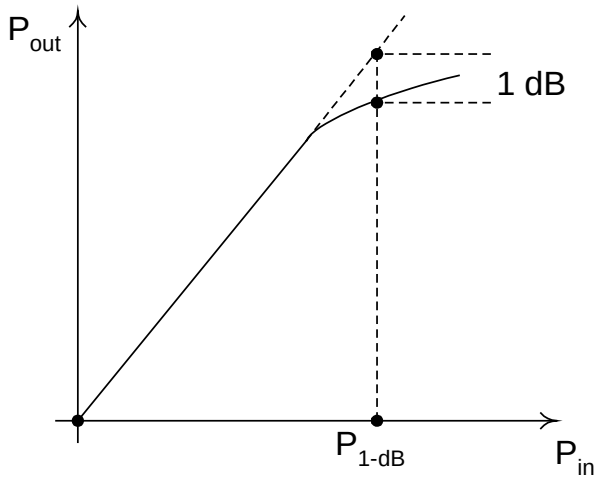

Fig. A.1 Definition of the 1-dB compression point

Intermodulation Distortion

Consider $x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$, then from equation (A.1):

$$\begin{aligned} y(t) = {} & \left(\alpha_0 + \alpha_2 A^2\right) + \left(\alpha_1 A + \frac{9\alpha_3 A^3}{4}\right)\cos(\omega_1 t) + \left(\alpha_1 A + \frac{9\alpha_3 A^3}{4}\right)\cos(\omega_2 t) + \\ & \left(\frac{\alpha_2 A^2}{2}\right)\cos(2\omega_1 t) + \left(\frac{\alpha_2 A^2}{2}\right)\cos(2\omega_2 t) + \left(\alpha_2 A^2\right)\cos((\omega_1 + \omega_2)t) + \\ & \left(\alpha_2 A^2\right)\cos((\omega_1 - \omega_2)t) + \left(\frac{3\alpha_3 A^3}{4}\right)\cos((2\omega_1 - \omega_2)t) + \left(\frac{3\alpha_3 A^3}{4}\right)\cos((2\omega_2 - \omega_1)t) + \\ & \left(\frac{3\alpha_3 A^3}{4}\right)\cos((2\omega_1 + \omega_2)t) + \left(\frac{3\alpha_3 A^3}{4}\right)\cos((2\omega_2 + \omega_1)t) + \\ & \left(\frac{\alpha_3 A^3}{4}\right)\cos(3\omega_1 t) + \left(\frac{\alpha_3 A^3}{4}\right)\cos(3\omega_2 t) \end{aligned} \tag{A.8}$$

The third order input intercept point IIP_{3i} is defined as the intercept point of the fundamental component with the third order intermodulation component, as shown in Fig. A.2. From the previous definition and from equation (A.8), we have:

$$(\alpha_1 A_{IIP3i}) = \left(\frac{3\alpha_3 A_{IIP3i}^3}{4}\right) \Rightarrow A_{IP3i}{}^2 = \frac{4}{3}\frac{|\alpha_1|}{|\alpha_3|} \tag{A.9}$$

The third order intermodulation distortion IM_3 is defined as:

$$IM_3 = \frac{3}{4}\frac{|a_3|}{|a_1|}A^2 = 3HD_3 \tag{A.10}$$

Note from equations (A.5) and (A.9) that:

$$\frac{A_{IIP3i}{}^2}{A_{1-dB}{}^2} = 9.195 \Rightarrow A_{IIP3i}(dB) \cong A_{1-dB}(dB) + 10 \tag{A.11}$$

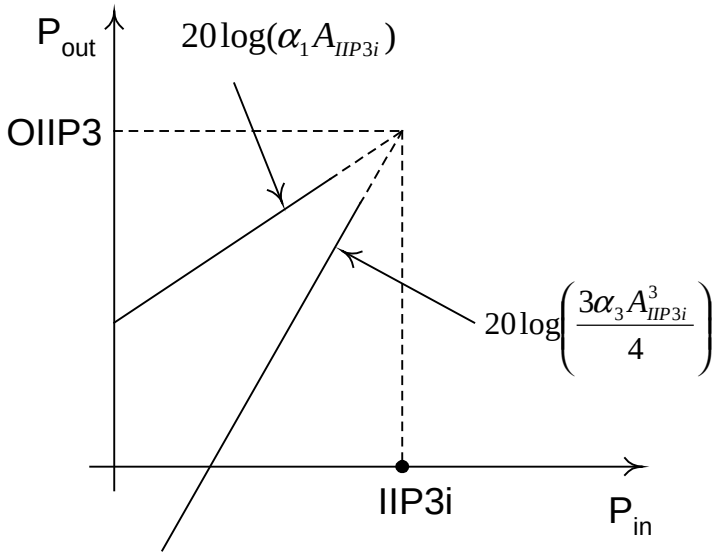

Fig. A.2 Definition of the third order intercept point

2. Dynamic Range

The are many definitions for the dynamic range. We define here the 1-dB compression dymanic range $DR_{1\text{-}dB}$ and the spurious free dynamic range (SFDR). The

SFDR is the difference, in dB, between the fundamental tone and the highest spur, which could be an intermdulation harmonic, in the bandwidth of interest.

$$DR_{1-dB} = P_{i,1dB} - P_{i,mds} \tag{A.12}$$

$$SFDR = \frac{2}{3}(IIP_{3i} - P_{i,mds}) \tag{A.13}$$

where $P_{i,mds} = -174dBm + 10\log B + NF$, $P_{o,mds} = P_{i,mds} + \alpha_1\big|_{dB}$

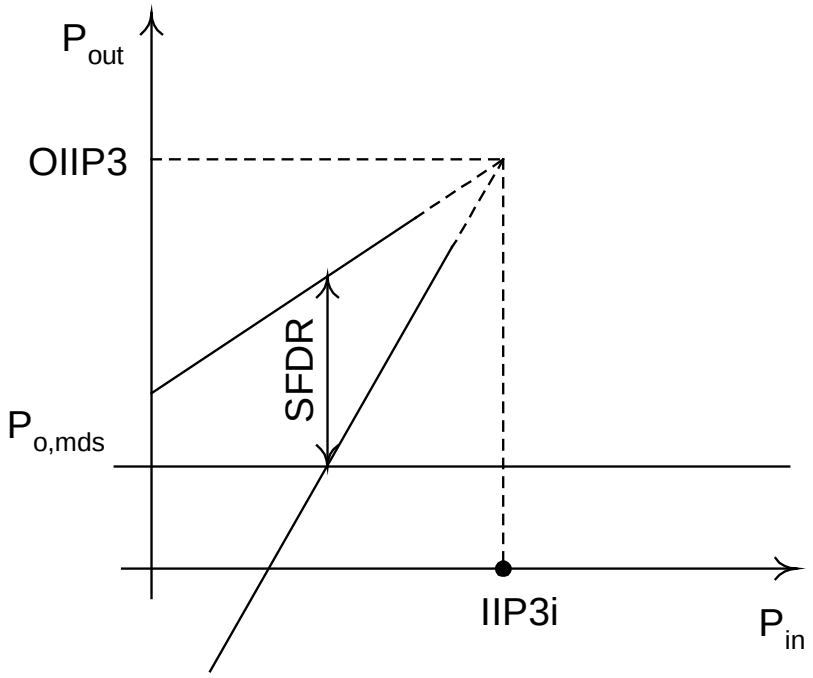

Fig. A.3 Definition of SFDR

Example

For a simple differential pair as shown in Fig. A.4.

$$I_0 = I_1 - I_2,\ I_{DC} = I_1 + I_2 \tag{A.14}$$

where $I_1 = \frac{I_{DC}}{2} + \frac{I_0}{2},\ I_2 = \frac{I_{DC}}{2} - \frac{I_0}{2}$

$$I_1 = \frac{\beta}{2}(V_{GS1} - V_T)^2,\ I_2 = \frac{\beta}{2}(V_{GS2} - V_T)^2, \text{ where } \beta = K_n \frac{W}{L} \tag{A.15}$$

$$V_{GS1} = V_T + \sqrt{\frac{2I_1}{\beta}},\ V_{GS2} = V_T + \sqrt{\frac{2I_2}{\beta}} \tag{A.16}$$

$$V_{GS1} - V_{GS2} = V_{in}^+ - V_{in}^- = v_d \tag{A.17}$$

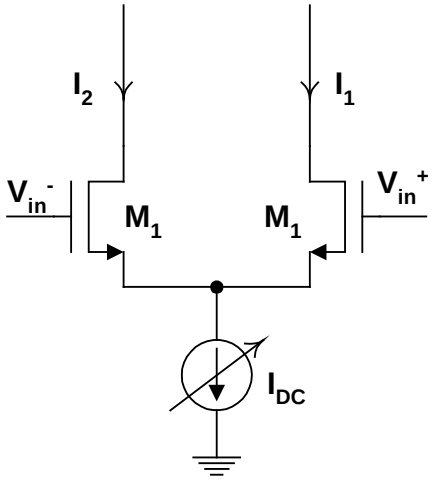

Fig. A.4 Simple differential pair

Substituting equtaion (A.16) in (A.17), we have:

$$v_d = \sqrt{\frac{2}{\beta}}\left(\sqrt{I_1} - \sqrt{I_2}\right) \tag{A.18}$$

Substituting equation (A.14) in (A.18), we have:

$$v_d = \sqrt{\frac{2}{\beta}}\left(\sqrt{\frac{I_{DC}}{2} + \frac{I_0}{2}} - \sqrt{\frac{I_{DC}}{2} - \frac{I_0}{2}}\right) \tag{A.19}$$

Squaring both sides and after some algebraic manipulation, we can write:

$$I_0 = v_d \sqrt{\beta I_{DC}} \left(1 - \frac{\beta v_d^2}{4 I_{DC}}\right)^{1/2} \tag{A.20}$$

Expanding I_o in a power series in terms of v_d, we have:

$$I_0 = \alpha_1 v_d + \alpha_3 v_d^3 + O(v_d^5) \tag{A.21}$$

where $\alpha_1 = \sqrt{\beta I_{DC}} = G_{in}$, and

$$\alpha_3 = \frac{1}{8}\sqrt{\beta I_{DC}}\,\frac{\beta}{I_{DC}} = \frac{1}{8}\frac{G_{in}}{(V_{GS} - V_T)^2} = \frac{1}{8}\frac{G_{in}}{V_{DSAT}^2}$$

According to (A.3b), HD_3 is given by:

$$HD_3 = \frac{1}{32}\frac{A^2}{V_{DSAT}^2} \tag{A.22}$$

According to (A.6), the 1-dB compression point A_{1-dB}^2 is given by:

$$A_{1-dB}^2 = k\frac{\alpha_1}{\alpha_3} = 8kV_{DSAT}^2 \Rightarrow A_{1-dB} = 1.077 \times V_{DSAT} \tag{A.22}$$

According to (A.9), the third order intercept point A_{IIP3i}^2 is given by:

$$A_{IIP3i}^2 = \frac{4}{3}\frac{\alpha_1}{\alpha_3} = 10.66 \times V_{DSAT}^2 \Rightarrow A_{IP3i} = 3.266 \times V_{DSAT} \tag{A.23}$$

According to (A.10), the third order intermodulation distortion IM_3 is given by:

$$IM_3 = \frac{3}{4}\frac{a_3}{a_1}A^2 = \frac{3}{32}\left(\frac{A}{V_{DSAT}}\right)^2 \tag{A.24}$$

According to the derivation in section 2.3.3, an expression for IM_3 of a psuedo-differential pair (removing the tail current source of Fig. A.4) can be obtained as:

$$IM_3 = \frac{3}{16}\frac{A^2\theta}{V_{DSAT}(1+\theta V_{DSAT})^2(2+\theta V_{DSAT})} \tag{A.25}$$

3. Cascaded Nonlinear Stages

Consider two nonlinear stages in cascade as shown in Fig. A.5. It can be shown that [84] the overall third order intercept point A_{IIP3} is given by:

$$\frac{1}{A_{IIP3}^2} \cong \frac{1}{A_{IIP3,1}^2} + \frac{G_1^2}{A_{IIP3,2}^2} \tag{A.26}$$

where $A_{IIP3,i}$ is the input IIP3 point of the i^{th} stage, and G_i is the gain of the i^{th} stage.

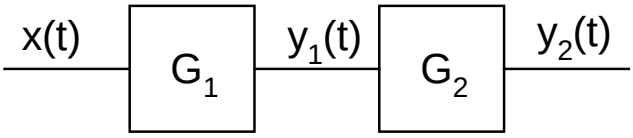

Fig. A.5 Cascaded nonlinear stages

Equation (A.26) can be generalized for more stages as:

$$\frac{1}{A_{IIP3}^2} \cong \frac{1}{A_{IIP3,1}^2} + \frac{G_1^2}{A_{IIP3,2}^2} + \frac{G_1^2 G_2^2}{A_{IIP3,3}^2} \tag{A.27}$$

4. Cadence Simulation

To simulate the 1-dB compression point or the two-tone intermodulation distortion of the differential amplifier, the setup shown in Fig. A.6 is used. Swept Periodic Steady State (SPSS) analysis simulation of SpectreRF is chosen. The input is applied through

PORT0. It is a power source and is called "**psin**" in "**analogLib**" library. The output resistance of the source is set as 50Ω. A physical resistance of 50Ω (not shown in Fig. A.5) should be placed in parallel with the source for matching purposes, since the resistance seen form the gate of the MOSFET transistor is infinity. The source type should be "**sine**" as shown in Fig. A.7. The input consists of two relatively close frequencies ($F_1=F_{in}$=10MHz,$F_2=F_{in}$+1MHz=11MHz) and their power levels are set equal to a design variable called $\mathbf{P_{in}}$ (make sure that the Amplitude and Amplitude2 fields are left empty). This is the variable that will be swept in the SPSS simulation.

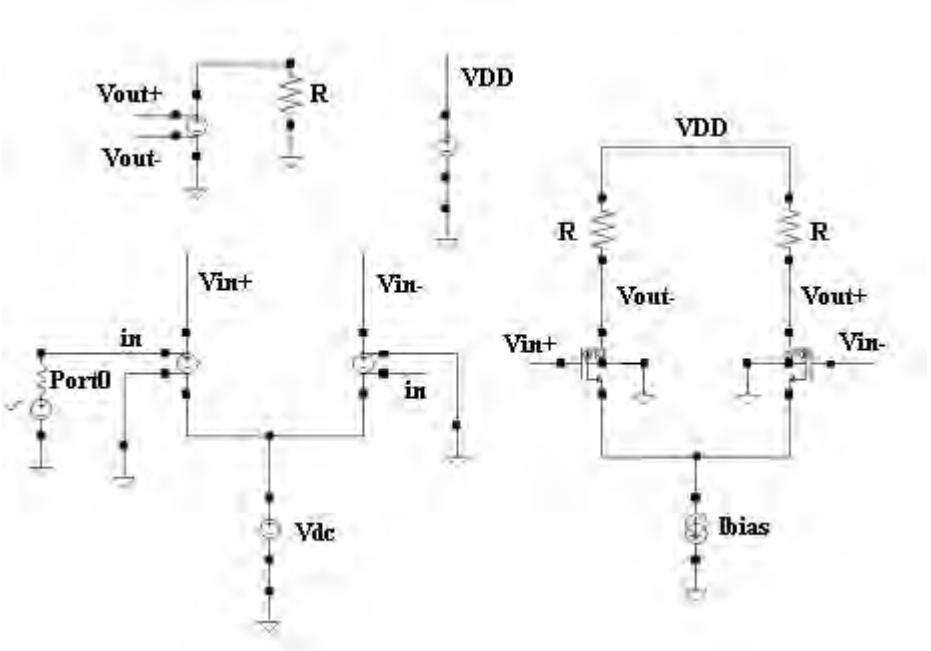

Fig. A.6 Swept periodic steady state (SPSS) simulation setup

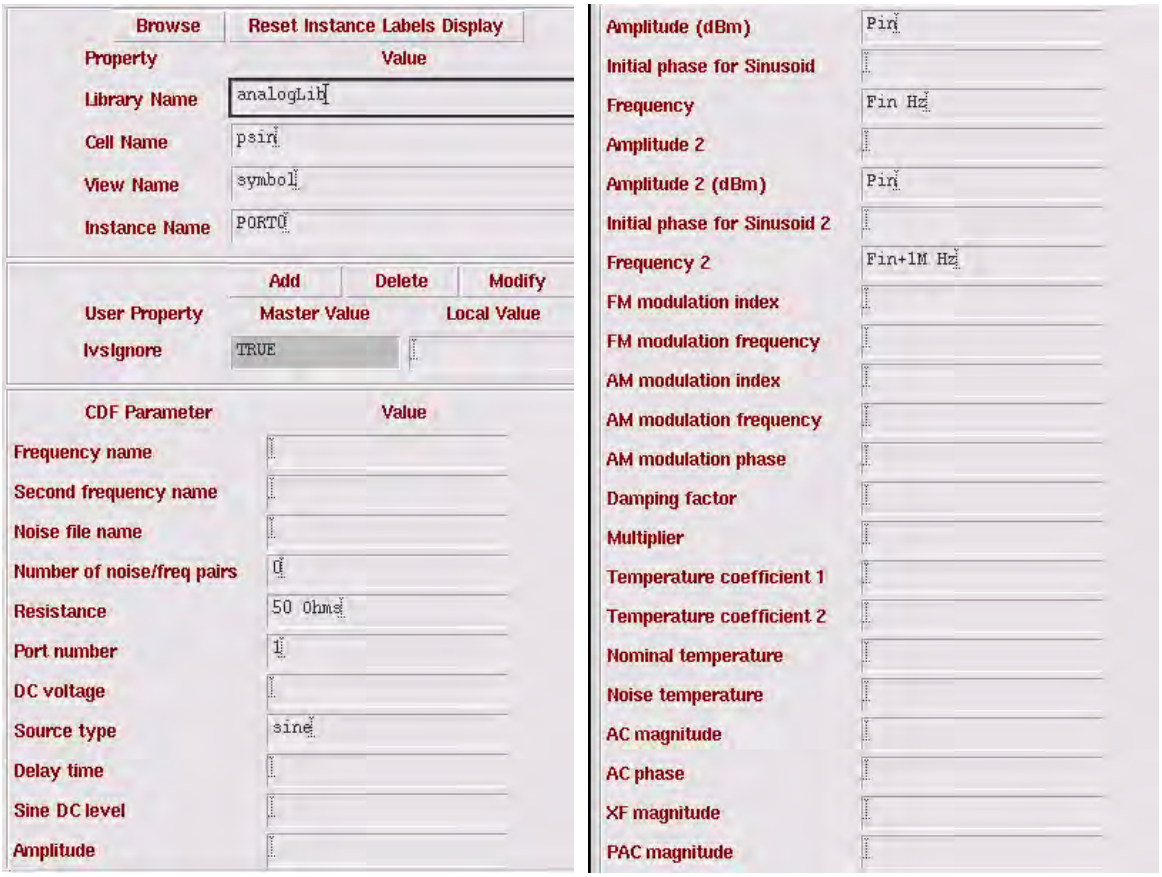

Fig. A.7 PORT0 setup

In the simulation window, select SPSS analysis. The **Fundamental (Beat)** frequency is the highest frequency common to all inputs shown in the **Fundamental Tones** section. In the sweep section, select "**variable**" to sweep $\mathbf{P_{in}}$ from –30dBm to 10dBm. Only the harmonics of interest (9,10,11,12) are saved to reduce the disk area required for saving, as shown in Fig. A.8.

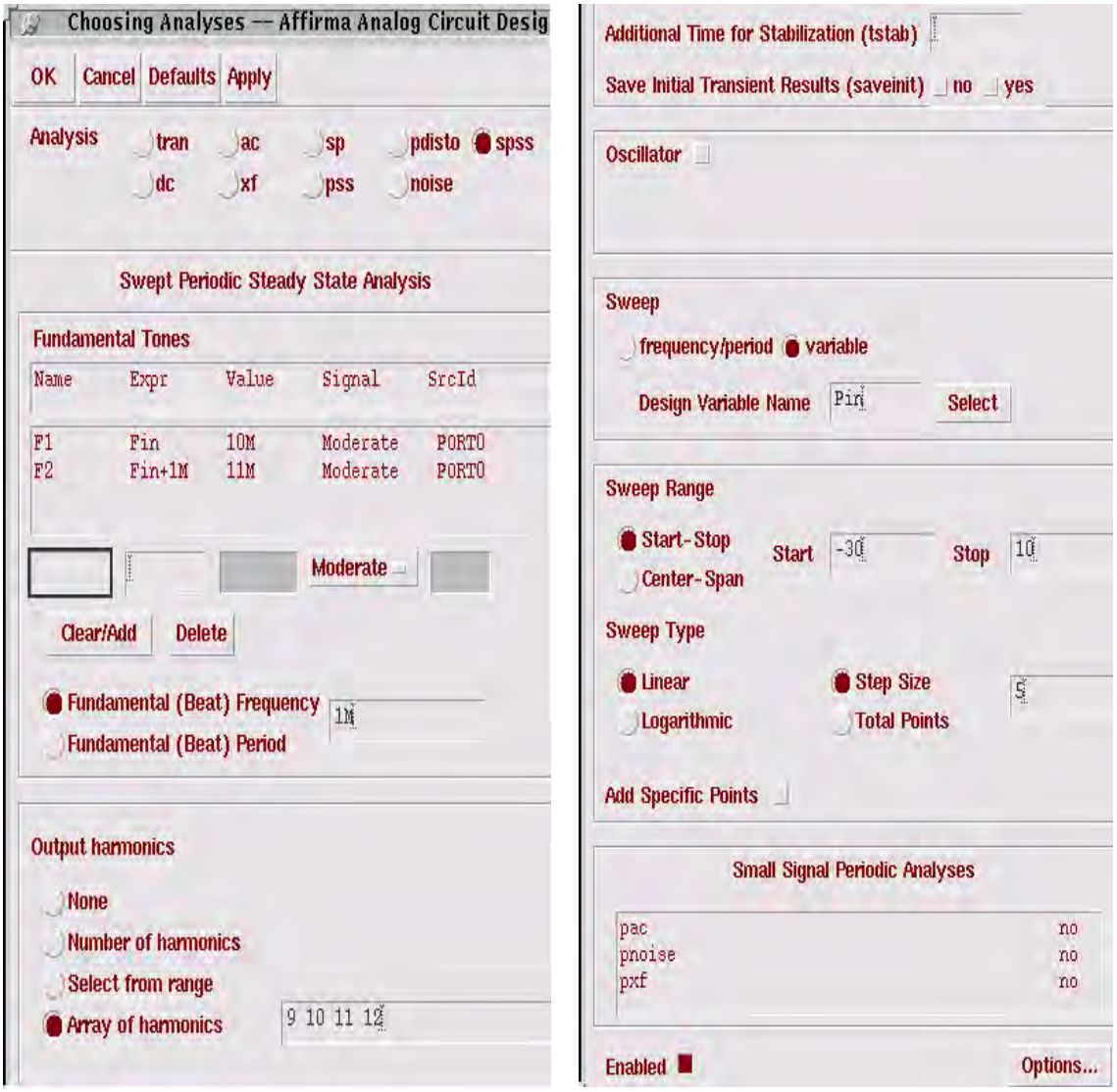

Fig. A.8 SPSS analysis setup

From "**Options**" button choose "**gear2only**" as the integration method. It is important to switch to "**flat**" netlisting to run SPSS. Select **Setup->Environment.** Set the netlist type as "**flat**". After running the simulation, you can display the IIP_3 plot from Analog Artist, select **Results->Direct Display->SPSS**. Setup the form as shown in Fig. A.9. The 1st order harmonic is at 10MHz and the 3rd order harmonic is at 9MHz.

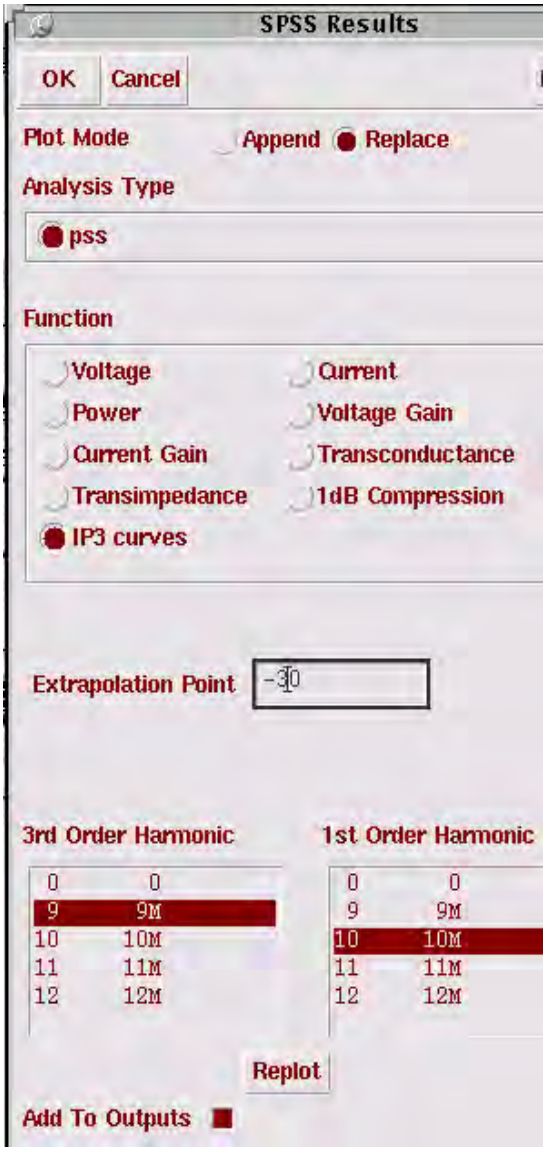

Fig. A.9 IIP3 results setup

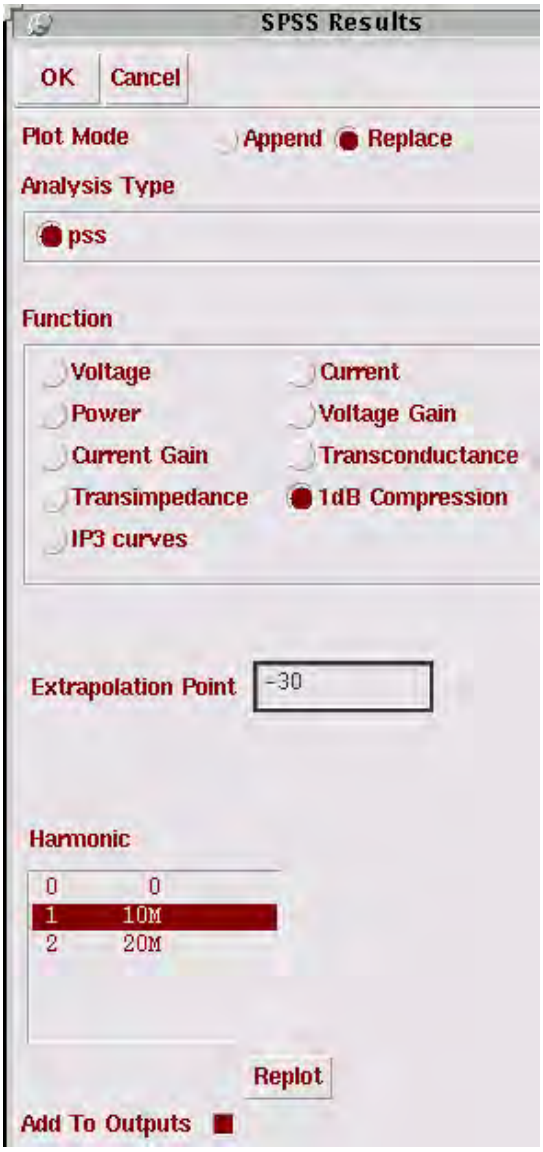

Fig. A.10 1-dB compression results setup

For the 1-dB compression point simulation only one frequency F_{in} is specified and the N**umber of harmonics** is set to 2. $\mathbf{P_{in}}$ is swept from –30dBm to 10dBm. The form of SPSS results is set as shown in Fig. A.10. The 1st order harmonic is at 10MHz. Select node V_{out} (of Fig. A.5). The 1-dB compression point plot should look like Fig. A.11. The 1-dB compression point is about –4.9dBm, compared to the theoretical value calculated

according to (A.22), that is –3.3dBm for our case of V_{DSAT}=200mV. The IIP_3 plot should look like Fig. A.12. IIP_3 is about 6.1dBm, which is very close to the theoretical value calculated according to equation (A.23), that is 6.3dBm for our case of V_{DSAT}=200mV.

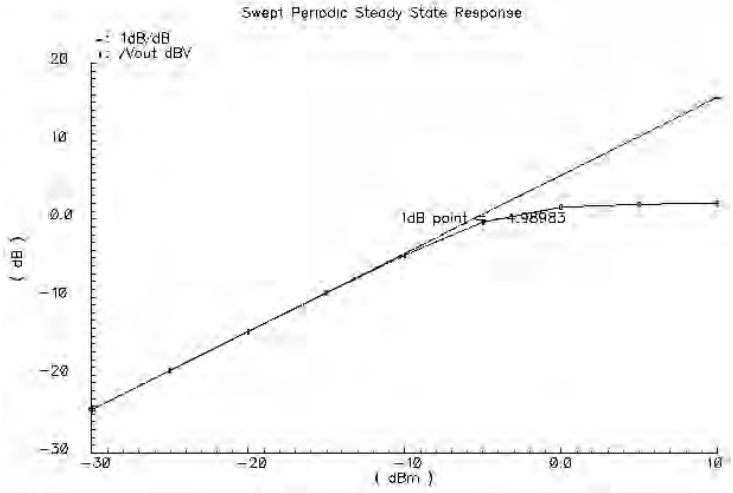

Fig. A.11 1-dB compression point plot

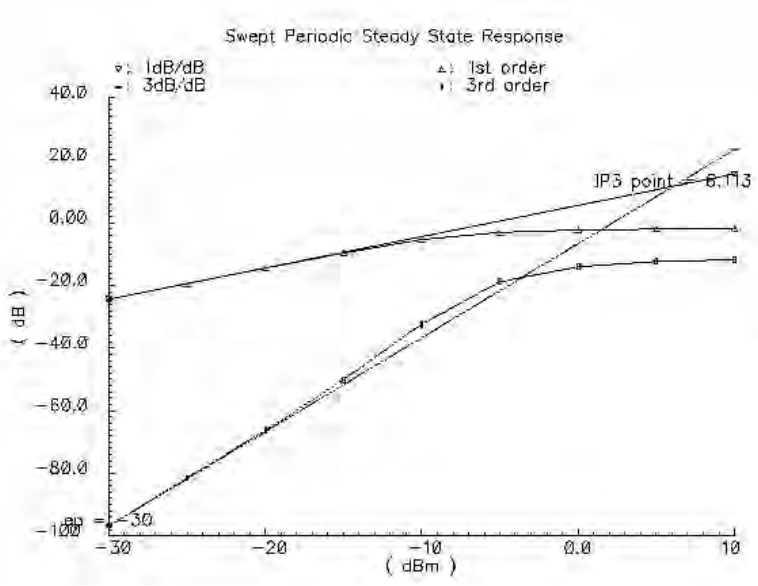

Fig. A12 IIP3 plot

Appendix B

As part of this dissertation, the following publications were generated.

[1] **Ahmed N. Mohieldin**, Ahmed Emira, and Edgar Sánchez-Sinencio, "A 100MHz, 8mW ROM-Less Quadrature Direct Digital Frequency Synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp.1235-1243, October 2002.

[2] **Ahmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A Low-Voltage Fully Balanced OTA with Common Mode Feedforward and Inherent Common Mode Feedback Detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp.663-668, April 2003.

[3] **Ahmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A 2.7V, 1.8GHz, 4th Order Tunable LC Bandpass Filter Based on Emulation of Magnetically-Coupled Resonators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, July 2003.

[4] **Ahmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "Nonlinear Effects in Pseudo-differential OTAs with CMFB," *submitted to the IEEE Transactions on Circuits and Systems.*

[5] A**hmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A Low-Voltage Fully Balanced OTA with Common Mode Feedforward and Inherent Common Mode Feedback Detector," *European Solid-State Circuits Conference*, *pp.191-194*, Florence, Italy, September 2002.

[6] **Ahmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "A 2.7V, 1.8GHz, 4th Order Tunable LC Bandpass Filter with ±0.25dB Passband Ripple," *European Solid-State Circuits Conference, pp.343-346,* Florence, Italy, September 2002.

[7] Ahmed Emira, **Ahmed N. Mohieldin**, and Edgar Sánchez-Sinencio, "A 100MHz, 8mW ROM-Less Quadrature Direct Digital Frequency Synthesizer," *European Solid-State Circuits Conference, pp.427-430,* Florence, Italy, September 2002.

[8] **Ahmed N. Mohieldin**, Ahmed Emira, and Edgar Sánchez-Sinencio, "A 2V 11Bit Incremental A/D Converter Using Floating Gate Technique," *Proceedings of the IEEE International Symposium on Circuits and Systems*, Scottsdale, Arizona, May 2002.

[9] **Ahmed N. Mohieldin**, Edgar Sánchez-Sinencio, and José Silva-Martínez, "Design Considerations of Bandpass LC Filters for RF Applications," *Proceedings of the IEEE Midwest Symposium on Circuits and systems,* Tulsa, Oklahoma, 2002.

[10] Mingdeng Chen, **Ahmed N. Mohieldin**, and José Silva-Martínez, "Linearized OTAs for High-frequency Continuous-time Filters: A Comparative Study," *Proceedings of the IEEE Midwest Symposium on Circuits and systems*, Tulsa, Oklahoma, 2002.

[11] José Silva-Martínez, Regina Origel, Adan Lopez, Siang Tong Tan, and **Ahmed N. Mohieldin**, "Analog Building Blocks for High Frequency Applications," *Proceedings of the IEEE 2nd Dallas Circuits and Systems Workshop on Low Power/Low Voltage Mixed-Signal Circuits and Systems*, Richardson, Texas, March 2001.

VITA

Ahmed Nader Mohieldin was born in Cairo, Egypt in 1974. He received the B.Sc. and M.Sc. degrees from the Electronics and Communications Department, Cairo University, Cairo, in 1996 and 1998, respectively. From July 1996 until December 1998, he worked as a teaching assistant at the same department. He has been a graduate student and research assistant in the Electrical Engineering Department of Texas A&M University in the Analog and Mixed-Signal Center since January 1999. He is presently working towards the Ph.D. degree. In Summer of 2000 he worked in the RFIC Design Group of Texas Instruments in Dallas as a design engineer for his internship. His research interests include analog and mixed-signal circuit design, wireless communication, and continuous-time filter design. He has been an IEEE Student Member since 2001. He can be reached through Dr. Edgar Sánchez-Sinencio, 318E Wisenbaker Engineering Research Center, Analog and Mixed Signal Center, Department of Electrical Engineering, Texas A&M University, College Station, Texas 77843-3128, USA.